# **Design Low Noise Digital Decimation Filter For Sigma-Delta-ADC**

Pramod Kumar Singh, Kanika Sharma

Deptt. Of Electronics Engg.

NITTTR, Chandigarh

misty.pksingh@rediffmail.com

Deptt. Of Electronics Engg.

NITTTR, Chandigarh

kanikasharma80@yahoo.com

Abstract-This paper focuses on the design of digital decimation filter for single bit Sigma-Delta A/D converter with medium oversampling ratio for the processing of audio and biomedical signal. A second-order single-stage sigma-delta ( $\Sigma$ - $\Delta$ ) modulator with single bit quantizer with oversampling ratio 96 workas a basic modulator. For hardware requirement, multiplier less CIC compensation FIR filter architectureused. Total three CIC compensation filter are used for decimation and filtering purpose. All filters are designed and simulated with MATLAB

#### Keywords-

ovesampling,downsamplingquantization noise, sigma-delta modulator, decimation filter, CIC compensation filter,MATLAB Tools.

Introduction-Each sampling period for the FIR and IIR digital filter require large number of multiply and accumulation operation. Nyquistrate ADC sample the analog input signal are  $f_s \ge 2f_b$ , where  $f_b$  is the highest frequency component of the input signal and fs is the sampling frequency. For avoiding the antialiasing we ensure that the filtered signal which does not have frequency components  $\geq$ f<sub>s</sub>/2.Hence the anti-aliasing filter should have a very narrow transition band[1]. High-resolution analog-to-digital conversion(ADC) based on Sigma-Delta modulation has become common place in many measurement applications including audio, biomedical, seismic and noisy environment sensing.

Sigma-Delta methods incorporating over sampling and noise shaping provide improved resolution over Nyquist- rate conversion methods and accuracy for time. However, this architecture requires both filtering and down sampling of the over sampled signal [2], or decimation filter. The modulator shapes the noise by shifting it towards the high frequencies the decimation filter takes the output sequence from the modulator, reduces the sampling freequency while suppressing high frequency quantization noise.

The overarching theme of these techniques has been to reduce the complexity of the multiplication to reduce the word length.. There are many techniques that use some form of sigma delta modulation or the like to improve the efficiency of the digital filtering operations. In this paper we thoroughly examine the design and synthesis of such techniques including general purpose short word length (SWL) DSP technique .

An alternative solution is to use gate level programmable devices such as field programmable devices arrays to perform digital filtering tasks . Anti aliasing filter must have a very narrow transition band which is not easy to realize[3]. Also the resolution which is not reducing the baseband quantization noise is suitable for a very low voltage converter. Reducing the base band quantizing noise is equivalent to increasing the effective resolution of the digital output[4]. Noise is reduce by using Low Pass Filter (LPF) or compensated CIC filter. Basics of Sigma - Delta Modulator -The simplest predictive modulator is the linear Delta modulator. This is pushing most of the in band noise outside signal frequency band to improve SNR. This is obtaining if signal transfer function is a LPF whereas most important noise transfer function is HPF. Above technique called noise shaping and can be easily and efficiently implemented by modifying the modulator. Here the integral of the input signal is encoded rather than the input signal directly [5]. Integration being a linear function does not affect system transfer function. The demodulation output feeded at the input of Delta modulator.

of Nyquist-rate converter low is This new system is called Sigma-Delta Modulator. Signal encoding with sigma-delta modulation work as an ADC and single bit coder so there is no longer a requirement for a conventional ADC, then here coder circuit are used[6,7]. Further no input interpolation is required in this setup as a signal passing through sigma-delta will be over sampled. To filtering operation for full precision filter coefficient where zero padded by R used to match the oversampling ratio of the Sigma-Delta modulator. Decoder circuit comprising cascade comb and base band filter where used to remove the quantization noise and aliases from the filter out put signal. However the output signal was in a multi bit format in all of theseschemes[8,9]. The output of Sigma-Delta Modulator is very high sampling rate. High frequency quantization noise is filter out it possible to reduce the sample rate. Minimize the amount of information for subsequent transmission (Storage or digital signal processing)[10].



## To Design Digital Filter

The efficient filter fall on two categories, the first is purpose of filtering which reduced sampling rate and quantization noise. The second is choice of filter topology and design of cascade integrator comb filter

## (A)Purpose of Filtering

Some basic tasks are to be performed in the digital filter sections:

(1)Remove shaped Quantization Noise- The  $\Sigma$ - $\Delta$  modulator is designed to suppress quantization noise in the baseband. Most of the noise is at above the base-band frequency. The digital filter is used to remove the quantization noise which is out of band. Thus remains a little amount of baseband quantization noise and the component of

band-limited input signal. So to Reduce the baseband quantization noise we have to increase the effective resolution of the digital output [4,2].

Best use of sigma-delta modulator provide good noise shaping at low OSR.As the OSR increase, the order of filter should be increases to maintain same frequency response when sampling rate is high noise move to high frequency and most of it lies above base band[10].

(2) Decimation or sample rate reduction: The output of the modulator is high sampling rate. This is a basic characteristic of Sigma-Delta modulators because they use the high frequency portion of the spectrum of the quantization noise. If high frequency quantization noise is filtered, then it is possible to reduce the sampling rate. It is not desirable to bring the sampling rate down to the Nyquist rate which minimizes the amount of information for subsequent transmission and processing [8,11].

## (B) Choice of Filter topology

There are a many factors that make it difficult to implement the digital decimation filter. The digital decimation filter is used as low frequency and sampling rate of the modulator is high [12].Thus, the decimation filter must perform very well to remove the excess quantization noise. This filter used for high quality audio conversion impose the additional constraint that the digital signal processing must perform its task without distorting the magnitude and phase characteristics of the input signal in the baseband.

# (1)Design of Cascade Integrator Comb Filter and Compensation Filter

The filter choice depends on the factors that make it difficult to implement the digital decimation filter. The sampling rate is high the decimation filter perform very well to remove the excess quantization noise. The comb filter is not  $\Sigma_{-\Lambda}$  modulator is at a very high very effective at removing the large volume of out of band quantization noise generated by Sigma-Delta Modulator. The most economical and simplest filter to reduce the input sampling rate is a CIC filter, such a filter does not require a multiplier because filter coefficients are all unity. Also the frequency response of the comb-filter can cause substantial magnitude drooping at the upper region of baseband. So for those applications which cannot tolerate this distortion, the comb-filter is being used in conjunction with one or more additional digital filter stages. The cascaded comb filter is used in this design because it was found that using more than two cascaded comb filter did not improve the trade of between signal to noise rate of the coded output and the OSR. The decoder for this structure was identical to the shown in Fig[2].



Cascade Integrated Comb filter

To perform the filtering operation full precision filter coefficient where zero padded by R to match the oversampling ratio of the sigma-delta modulator. Decoder circuit comprising cascade comb and base band filter where used to remove the quantization noise and aliases from the filter out put signal. In all of these schemes the output signal was in a multi bit format.

#### (2) Mathemetical Model --

The comb filter operation is equivalent to rectangular window finite impulse response filter (FIR). The comb filter must be used in conjunction with one or more additional digital filter stages. A comb filter of length K is a FIR filter with all K coefficients equal is one. The transfer function of a comb filter is

$$H(Z) = \frac{Y(Z)}{X(Z)} = H_1(Z)Hc(Z) \dots (3)$$
  
Where  $H_1(Z) = \left[\frac{1}{1-Z^{-1}}\right]$  and  
 $H_c(Z) = \left[1-Z^{-K}\right]X(Z)$ 

We generalize equation number (3) for N number of integrator comb filter pairs, and R is the rate change factor. The equivalent time domain impulse response of CIC filter can be viewed as a cascade of N rectangle pulses[13]. Each rectangular pulse has RM taps, then equation (3) becomes

$$H(Z) = \frac{Y(Z)}{X(Z)} = H_1^N(Z) H_C^N(Z^R) \dots (4)$$

To overcome the magnitude drop, a FIR filter that has a magnitude response that is the inverse of the CIC filter can be applied to achieve frequency response correction. Such filters are called compensation filter[14]. The compensation filter follows the CIC filter for data rate down conversion. The compensation filter always operates at the lower rate in a rate conversion design[15].Now, since the comb filter will be followed by an K: 1 decimator, the differentiation function can be done at the lower rate.

The magnitude response of an multi-stage CIC filter at high frequency( $f_s$ ).

$$|H_1(f)| = \left| \frac{\sin(Nt\pi)}{\sin(\frac{\pi f}{R})} \right|^N$$
.....(5)

. .....

N=no. of stage of CIC filter

for large number of stage ,the CIC filter frequency response does not have a wide,flat pass band.Overcome the magnitude droop,a filter that has a magnitude response is the inverse of the CIC filter can be applied to achieve frequency response correction is called CIC compensation filters.The compensation filter operates at the lower in a rate conversion design it achieve a more efficient hardware solution.Magnitude response of the compensation filter is the inverse of CIC is[4,13].

$$|H_{C}(f)| = |MR \frac{\sin(f\pi/R)}{\sin(\pi Mf)}| \qquad N = |\frac{\pi Mf}{\sin(\pi Mf)}| \qquad N$$
$$= |\sin c^{-1} (Mf)|^{N} \qquad \dots \dots \dots (6)$$

In this equation, M is the differential delay it is limited to 10r2.

Response of above function is plotted for CIC filter at low frequency  $f_s/R$ ,here compensation filter operates at half of low frequency  $f_s/R$ . For the compensation filters to avoid aliasing, the cut-off frequency( $f_c$ ) is  $f_c < (f_s/R)/4$ . The frequency response of above filter is shown in Fig[3],and table-1 shows the comparative study of filter.





TABLE-1

Filter with decimation factor $= 96$	Magnitude (dB) of Passband droop at Normalized					
	Frequency for( $f_s$ )					
	0.005	.010	.0125	.0150	.0175	.020
Single stage CIC filter	69.79	68.73	67.61	65.12	62.79	58.23
Compensated CIC with one FIR filter	37.21	37.21	36.73	32.11	16.62	-43.18
stage						
Compensated CIC with two FIR filter	37.21	37.21	36.83	33.13	5.63	-42.21
stage 3						

#### Matlab Simulation-

To determine filter characteristic and performance one behavior model of second order Sigma Delta ADC designed and simulated using MATLAB- SIMULINK. Through MATLAB simulation it was found that short wavelength filter has a superior performance than the others that is single bit filter.



Fig. [4] magnitude response of CIC + compensation filter and it's noise

**Result**-The output of modulator is a signal bit data applied into decimation filter and it simulate in MATLAB.The magnitude and noise spectrum of CIC compensation filter is desirable and comparative study is given in table-2. From recorded data the pass-band is very sharp in CIC compensation filter and noise is also reduced by 5.8% [14,15].Logic analyzer output is shown in table-3.

#### TABLE-2

Filter type	Pass band	Magnitude	Stop band	Pass band	SNR(db)
	ripple(dB)	of pass	attenuation(dB)	edge f/R	
		band (dB)			
CIC filter	.071	80.3	91.6	.42	98.07
CIC	.048	90.5	91.5	.22	104.08
compensation					
filter					

#### TABLE-3

#### **Output value of sine wave**

input	Sign	Binary form	Decimal	Analog
parameters	bit		Equivalent	Equivalent
				(V)
V <sub>in</sub> =1.2	0	10010000110100	09268	+.3188
volt (p-p),	1	10000011001001	08393	- 0.3035
	0	10010101001000	09544	+0.3469
Frequency =3 kHz	1	10000111001010	08650	- 0.3165
	0	11101100101000	15144	+0.5532
	1	11111011010100	16084	- 0.5626

**Conclusion**-The Sigma-Delta modulator and CIC compensation digital filter reduce noise this also gives overall 14 bit resolution[16] .The discrete output value coincide with sine wave then noise and buffering problem is reduce in this filter. Output noise is also eliminated by using narrow - band filter.

# **Reference-**

[1] Subir Kr. Maity, Himadri Sekhar Das "FPGA Based Hardware Efficient Digital Decimation Filter for Sigma Delta ADC" International Journal of Soft Computing and Engineering(IJSCE), Vol-1, Issue-6, Jan 2012.

[2] Sangil Park, Principles of Sigma Delta Modulation for Analog to Digital Converters .Motorola Digital Signal Processors.
[3] S. R. Norsworthy, R. Schreier, and G. C. Temes, Delta-Sigma Data Converters: Theory, Design, and Simulation. Piscataway, NJ: IEEE Press, pp. 381, 1997.

[4]Geerts, Y., Steyaert, M.S.J., Sansen, W.M.: A 3.3-V, 15-bit Delta-Sigma ADC with a Signal Bandwidth of 1.1 MHz for ADSL Applications. IEEE J. Solid-State Circuits 34, Vol. 7,927–936, 1999.

[5] P. W. Wong, "Fully sigma-delta modulation encoded FIR filters," IEEE Transactions on Signal Processing, vol. 40, no. 6, pp. 1605–1610, 1992.

[6] C. L. Chen and A. N. Willson, "Higher order  $\Sigma$ - $\Delta$  modulation encoding for design of multiplierless FIR filters," Electronics Letters, vol. 34, no. 24, pp. 2298–2300, 1998.

[7] S. Kershaw, et al., "Realisation and Implementation of a Sigma-Delta Bitstream FIR filter," IEE Proceedings— Circuits, Devices and Systems, vol. 143, pp. 267– 273, 1996.

[8] T. D. Memon, P. Beckett, and Z. M. Hussain, "Analysis and design of a ternary FIR filter using sigma delta modulation," in Proceedings of the IEEE 13th

InternationalMultitopicConference(INMIC'09),pp. 476–480,December2009.

[9] Tayab Memon, Paul Beckett, Amin Z.Sadik " Sigma-Delta Modulation Based Digital Filter Design Technique in FPGA" International Scholarly Research Network ISRN Electronics, pp. 10 Vol-2012,

[10] C. Dick and F. Harris, "High-Performance FPGA Filters using Sigma-Delta Modulation Encoding," in Proceedings of the IEEE International Conferences on Acoustics, Speech, and Signal Processing (ICASSP '99), pp. 2123– 2126,1999.

[11] A. C. Thompson, Z. M. Hussain, and P. O'Shea, "A single-bit narrow-band bandpass digital filter,"Australian Journal of Electrical and Electronics Engineering, vol. 2, no. 1, pp. 31–40, 2005.

[12] J. C. Candy, "Decimation for sigma delta modulation," IEEE Transactions on Communications, vol. 34, no. 1, pp. 72–76, 1986.

[13] Vishal Awasthi, Krishna Raj ," A New Approach to Design an Efficient CIC Decimator Using Signed Digit Arithmetic,"World Academy of Science, Engineering and Technology International Journal of Electrical, Computer, Electronics and Communication Engineering Vol:7, No:11, 2013

[14]Understanding CIC Compensation Filters, Application Note 455 http://www.altera.com/literature/an/an455.pdf.

[15]Vishal Awasthi, Krishna Raj,"Application of Hardware Efficient CIC Compensation Filter in Narrow Band Filtering,"World Academy of Science, Engineering and Technology International Journal of Electrical, Computer, Electronics and Communication Engineering Vol:8, No:9, 2014.

[16]Mohammed Arifuddin Sohel, K. Chenna

Kesava Reddy, Syed Abdul Sattar, "Design of Low Power Sigma Delta ADC" International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.4, August 2012.