An Efficient Implementation Of MIMO OFDM Transceiver on FPGA

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Abstract: Orthogonal frequency division multiplexing (OFDM) is a popular method for high data rate wireless transmission. MIMO OFDM has many promising features which allow wireless devices to communicate at a higher data rate with reduced errors and hardware complexity. This paper describes a design and implementation of a baseband Orthogonal Frequency Division Multiplexing (OFDM) transceiver utilizing Multiple Input Multiple Output (MIMO) signal processing for increased data rate. Orthogonal frequency division multiplexing (OFDM) has become a popular technique for transmission of signals over wireless channels. OFDM may be viewed as using many slowly-modulated narrowband signals rather than one rapidly-modulated wideband signal. This work describes how implement an OFDM modem on FPGA using VHDL for a 31 subcarrier (channels) OFDM system using 64 points radix-4 FFT time decimation, a CORDIC implementation to perform the butterfly calculus, and each channel modulation will use a 4-QAM constellation. The system is divided in a transmission section and a reception section.

Keywords: Orthogonal Frequency Division Multiplexing, Multiple Input Multiple Output, VHDL, FPGA

1. Introduction

The OFDM technique (Orthogonal Frequency Division Multiplexing) has been used in the last years in applications that require a huge transmission rate like wireless network (Wi-Fi 802.11), DVB (Digital Video Broadcasting) and DAB (Digital Audio Broadcasting). The main aim of all new wireless communication technique is to get maximum throughput in the given bandwidth with the minimum error[1]. In all the above cases, one needs to implement an integrated circuit (IC) that performs the necessary chip functions. For prototyping circuits FPGA is better choice than using ASIC (application Specific Integrated Circuit), CUSTOM or SEMICUSTOM. FPGA implementations because avoid the:

- Initial costs;
- Great development time and the inherent risk of conventional ASIC.

So, in this way, the development of high advanced techniques of digital data transmission and the actual FPGA stage of integration make possible the building all the circuits that compounds a digital communication systems in an unique chip. To make use of this modern technologies of data transmission, it is necessary the development efficient techniques of digital modulation. The OFDM is the biggest utilized recently, principally, because of it use the efficient FFT to do the modulation.Orthogonal frequency-division multiplexing (OFDM) is the technique of choice in the digital broad-band applications, which divides a channel with a higher relative data

rate into several orthogonal sub-channels with a lower data rate. This very special feature of OFDM technique attracts the new generation of communication, which in mobile communication terminology called as "4th generation technology". This paper is an approach towards reducing the complexity MIMO OFDM design which will be implemented on FPGA KIT.

2. Survey Work

A few research work have been conducted to explain the concept of MIMO OFDM. OFDM provides efficient utilization of the given spectrum and supports high data rates without the use of complex equalizers. When combined, MIMO OFDM systems can provide data rates of several Mbps without the use of complex hardware or large bandwidth. Keeping these advantages in view MIMO OFDM has been selected as the physical layer scheme for the latest WLAN standard 802.11n [2]. However hardware implementation of the new scheme includes many challenges which need to be addressed. [3] describes these challenges and also provides solutions to few. In [4] a basic design for 802.11a using MIMO is proposed and practical limitations of MIMO are shown. In [5] a receiver for the new standard is explained. In [6] a FPGA based design is considered for 802.11n physical layer which also gives performance parameters for various combinations. In this paper a low complexity MIMO OFDM design is implemented on a Spartan 6 FPGA. The system is designed using Xilinx System Generator for Simulink. Various alternatives for some blocks in the design are investigated to get minimum resource utilization along with optimum performance.

3. System Design

Following figure shows the block diagram for MIMO OFDM transceiver.



Fig. 1. Block diagram of a MIMO OFDM transceiver

3.1 Convolution Encoding

In telecommunication, convolution code is a type of errorcorrecting code in which

- •Each m-bit information symbol (each m-bit stream) to be encoded is transformed into an nbit symbol, where m/n is the code rate (n>m).
- •The transformation is a function of the k information symbols.

Coding is a technique where redundancy is added to original bit sequence to increase the reliability of the communication.

To convolutionally encode data, start with a k memory registers, each holding one bit input, All memory registers start with a value of zero, unless otherwise specified, The encoder has n modulo-2adders (a modulo 2 adder can be implemented with a single Boolean XOR gate, where the logic is: 0+0 = 0, 0+1 = 1, 1+0 = 1, 1+1 = 0), and n generator polynomials, one for each adder.

There are three parameters which define the convolotional code:(a) **Rate** : Ratio of the number of input bits to the number of output bits. In this example, rate is 1/2 which means there are two output bits for each input bit.

(b) **Constraint length** : The number of delay elements in the convolutional coding. In this example, with K=3 there are two delay elements.

(c) **Generator polynomial** : Wiring of the input sequence with the delay elements to form the output. In this example, generator polynomial is [7,5]8=[111,101]2. The output from the 78=1112 arm uses the XOR of the current input, previous input and the previous to previous input. The output from the 58=1012 uses the XOR of the current input and the previous to previous input.



3.2 Mapper

The mapper converts input data into complexed valued constellation points, according to a given constellation. Typical constellations for wireless applications are, BPSK, QAM, and 16 QAM, see Figure 3. In Figure 3, I is the in phase component

and Q is the quadrature component. The amount of data transmitted on each subcarrier depends on the constellation, e.g. BPSK and 16QAM transmit one and four data bits per subcarrier, respectively. Which constellation to chose depends on the channel quality. In an high interference channel a small constellation like BPSK is favorable, since the required signal to noise ratio (SNR) in the receiver is low, whereas in a low interference channel a larger constellation is more beneficial due to the higher bit rate.

3.3 Parser

A MIMO wireless system includes a transmitter that has a transmitter having a parser that parses a bit stream into multiple spatial data streams and multiple interleavers corresponding to the multiple spatial data streams, where each interleaver interleaves the bits in the corresponding spatial data stream by performing multiple column rotation to increase diversity of the wireless system. The MIMO wireless system also includes a receiver that has deinterleavers that deinterleaves spatial bit streams transmitted by the transmitter.

3.4 IFFT

The output of this parser is fed to the IFFT block. The Inverse Fast Fourier Transform (IFFT) transforms the signals from the frequency domain to the time domain. Guard interval section is added at the last block of transmitter design. And then it is send to the receiver.

At the receiver side reverse of all these blocks is arranged in reverse order. Like remove guard interval is added as a first block and so on.

4. Module Design

The black box view of the MIMO OFDM system is shown Below.



Fig.3 Black box view of MIMO OFDM

5. Result

The MIMO OFDM design were simulated in Modelsim 6.6c and synthesized using Xilinx ISE 13.1i. The simulation results of 31 channels modulated to 4-QAM by an IFFT of 64 points are shown in Figure below. Table 1 shows the device utilization report and Table 2 gives comparison of device utilization between my work and [10]

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Fig.4 Simulation result of MIMO OFDM

Table-1 shows the hardware used for this project

Logic	Used	Availabl	Utilizati
Utilization		е	on
Number of slice	793	54576	1%
Register			
Number of	1112	27288	4%
slice			
LUTs			
Number of	744	1161	64%
fully used LUT-			
FF Pairs			

Table-1

Table-2 shows the comparison of hardware used.

G Slice Logic	My Work	Work Done				
Utilization		by [10]				
Number of Slice	793	8357				
Registers						
Number of Slice	1112	5246				
LUTs						
Table-2						

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