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Implementation of Adaptive Equalizer using FPGA

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Abstract: The quality of transmitted channel is deteriorated by channel imperfections. This results in high bit error rate at the receiver which in turn makes recovering the original signal difficult. Channel response is dynamic in nature and therefore to decrease bit error rate, adaptive equalizer is generally used at receiver end. The purpose of this paper is to present the FPGA implementation of adaptive equalizer.

Keywords: Channel imperfection, Adaptive equalizer, bit error rate

1. Introduction

Signal is transmitted from one point to another via communication channel.This acts as a medium for signal to propagate from transmitter to receiver. Decoder is used at the receiver end decoder to recover the original signal.

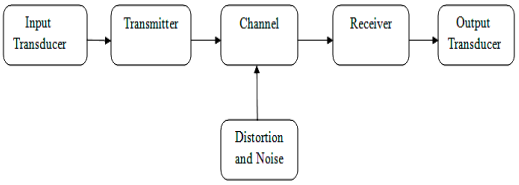

Fig.1The basic communication model

The channel have different characteristics like channel, phase distortion, signal attenuation,bandwidth etc. These characteristics degrades the transmitted signals at some measure. The aim of the receiver is to recover the original symbols without error, the distortions or inter-symbol, interference (ISI) caused by the channel, noise and other sources are tried to be minimized. Channel imperfections like amplitude and phase dispersion are removed by equalizers which results in the interference of the transmitted signals with one another. In most of the digital communications applications, the channel transfer function is not known at enough level to incorporate filters to remove the channel effect at the transmitters and receivers. Generally channel response is time varying and an equalizer must be designed which could track these changes. An adaptive equalizer could do this. Various adaptation algorithms have been proposed in literature, but due to its simplicity and less implementation complexity, least mean square (LMS) algorithm has been used for the proposed design.

II. BASICS OF EQUALIZATION PROCESS

Equalizer generates the inverse characteristics of the channel and combination of channel and equalizer results in a flat frequency response and linear phase. To compensate for the distortions, the adaptive equalizer use training and decision directed modes [11]. The general structure of the adaptive filter as [2] shown in Fig.2.

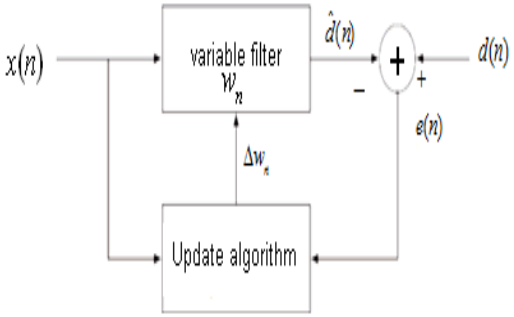

Fig.2 Adaptive filter

The input signal is the sum of a desired signal $d(n)$ and interfering noise v (n)

$$x(n) = d(n) + v(n) \quad (1)$$

The variable filter has a Finite Impulse Response (FIR) structure. For such structures the impulse response is equal to the filter coefficients. The coefficients for a filter of order p are defined as

$$w_n = [w_n(0), \quad w_n(1), \quad ..., \quad w_n(p)]^T \quad (2)$$

the error signal or cost function is the difference between the desired and the estimated signal

$$e(n) = d(n) - \hat{d}(n) \quad (3)$$

The variable filter estimates the desired signal by convolving the input signal with the impulse response. In vector notation this is expressed

$$\hat{d}(n) = w_n * x(n) \quad (4)$$

Where

$$x(n) = [x(n), \quad x(n-1), \quad ..., \quad x(n-p)]^T$$

(5)

is an input signal vector. Moreover, the variable filter updates the filter coefficients at every time instant

$$w_{n+1} = w_n + \Delta w_n \qquad (6)$$

Where Δw_n is a correction factor for the filter coefficients.The adaptive algorithm generates this correction factor based on the input and error signals. This paper presents the comparison of some of the channel equalization techniques. The paper also presents FPGA implementation of Fractionally Spaced Equalizer.

III. FPGA IMPLEMENTATION OF ADAPTIVE EQUALIZER

For implementing the proposed fractionally spaced equalizer, Xilinx 9.2i software has been used. VHDL code has been generated using system generator tool and resource and power utilization have been calculated using ISE software.

Table 1: Resource Utilization for the Targeted FPGA

Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	2,222	67,584	3%
Number of 4 input LUTs	1,060	67,584	1%
Logic Distribution			
Number of occupied Slices	1,645	33,792	5%
Total Number of 4 input LUTs	1,981	67,584	2%

Table 1 shows the resource utilization. Results show that the proposed design has very less resource utilization.

IV.CONCLUSION

Adaptive equalizers are used to generate the reverse characteristics of the channel and has the adaptation property, i.e. capability to track the changer in channel characteristics. In this paper a fractionally spaced equalizer has been implemented on an FPGA. Fractionally spaced equalizes have better equalization capability as compared to conventional equalizers. Xilinx 9.2i software has been used to synthesize the design and VHDL code has been generated using System Generator tool.

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