Design and simulation of Parallel circuit class E Power amplifier

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Abstract: Parallel circuit Class E amplifiers are topology variant of the class E amplifiers, in which the transistor is made to work as switch. The current and voltage at the transistor are made 180^{o} out of phase by using load network and biasing circuit. Hence the power dissipation is decreased and the efficiency of the amplifier is increased. This paper presents parallel circuit class E amplifier design and simulation in ADS 2011 tool for C band applications at 5 GHz .The single stage and two stage amplifiers are designed using the standard design equations with input, output and inter stage matching.

Keywords: Parallel circuit Class E amplifier, Two stage parallel circuit class E amplifiers, power added efficiency (PAE), drain efficiency (η), third order intermodulation, 1 dB gain compression.

1. Introduction

In modern portable two-way radios and cellular base stations power efficiency is the key requirement in the design of power amplifier to provide a long period and energy efficiency communication by decreasing power consumption. At the same time, the requirement for the cooling system could be reduced. The class E power amplifier is a promising candidate for a high efficiency power amplifier. The switched-mode Class E tuned power amplifiers with a shunt capacitance have found widespread application due to their design simplicity and high efficiency operation [1]. In the Class E power amplifier, the transistors operates as an on-to-off switch and the shapes of the current and voltage waveforms provide a condition when the high current and high voltage does not overlap simultaneously that minimize the power dissipation and maximize the power amplifier efficiency. Such an operation mode can be realized for the tuned power amplifier by an appropriate choice of the values of the reactive elements in its output matching circuit [2].

However, such a circuit schematic when a shunt capacitance and a series inductance can provide ideally 100-percent DC-to-RF efficiency is not a unique. The same results can be achieved using the circuit configuration with parallel circuit consisting of a parallel capacitance and a parallel inductance with an additional series filtering circuit to provide high level of harmonic suppression [4]. The generalized analysis of such a switched-mode power amplifier with calculation of voltage and current waveforms and some graphical results firstly was done by Kozyrev [3]. The circuit schematic, required waveforms, phase angles and values of the circuit elements differ from well-known types of the Class E power amplifiers. Therefore, the presented switched-mode tuned power amplifiers with parallel resonant circuit can be considered as a new subclass of switched-mode tuned Class E power amplifiers.

2. Parallel Circuit Class E Amplifier

The load network of parallel class E amplifier consists of shunt capacitor C_p, shunt inductor L and filter L_s-C_s and the load resistor. The shunt capacitor plays an important role in making the transistor to work as switch, the L_f -C_f filter is used to shape the output waveforms.

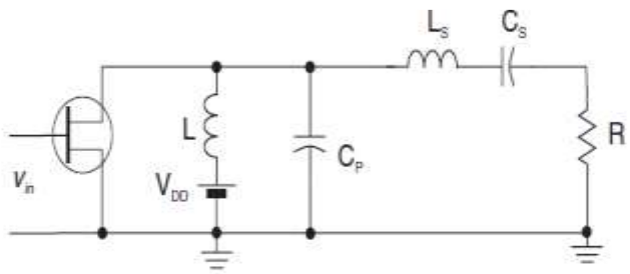

Figure 1: Parallel circuit class E power amplifier circuit

The transistor used is P-HEMT ATF36077 which operates at 2 GHz to 12 GHz and has drain capacitance of 0.05pF. Optimum resistance is required to make the load network elements drive the circuit such that current and voltage does not exist simultaneously at transistor.

For 50% duty cycle, the resistance value is calculated by:

$$R = 1.365 * \frac{V_{dd}^2}{P_{output}} \quad \text{(i)}$$

Where V_{dd} is bias voltage at drain of transistor, P_{out} is output power value to which amplifier is designed, ω is the angular frequency to which amplifier is designed.

The parallel capacitor which plays an important role in making the transistor work as switch, its value is given by:

$$C = \frac{0.685}{2 * \pi * f * R} \quad \text{(ii)}$$

The value of shunt inductor is given by:

$$L = 0.732 * \frac{R}{2 * \pi * f} \quad \text{(iii)}$$

The series filter L_s and C_s is determined by:

$$L_s = \frac{Q * R}{2 * \pi * f} \quad \text{(iv)}$$

$$C_s = \frac{1}{2 * \pi * f * R * Q} \quad \text{(v)}$$

The calculated load network values are given by:

R=30.7125 Ohm

C= 0.7099 pF

L=0.7156 nH

L_f=1.003027 nH

C_f= 1.01015pF

The drain and gate bias voltage are selected at the points where transistor is in saturation region. Drain voltage of 1.5 Volts and gate voltage -0.2 Volts are applied to the transistor.

3. Matching Network Design

Matching is important in amplifier to obtain maximum power at the load and reduce the power reflection at input and output. L-type matching network is chosen as the circuit is simpler and offers less reactance values. The input impedance Z_{11} is found at the input of the amplifier, its value is matched to 50 Ohm at the input using smith chart. The output impedance Z_{22} is found at the load and using smith chart, its value is matched to 50 ohm.

4. Two Stage Parallel Circuit Class E Amplifier

Two stage amplifier is designed with inter stage matching network. The first stage and second stage amplifier is designed similar to above said procedure and inter stage matching is done by finding the impedance at the end of first stage and at the input of second stage.

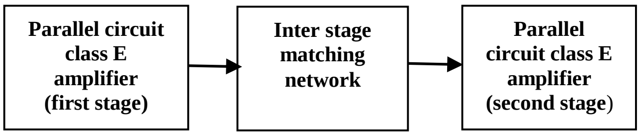

Figure 2: Block diagram of 2 stage parallel class E amplifier

5. Simulation Results

To verify the bias current and voltage values the transistor is simulated using FET curve tracer set up.

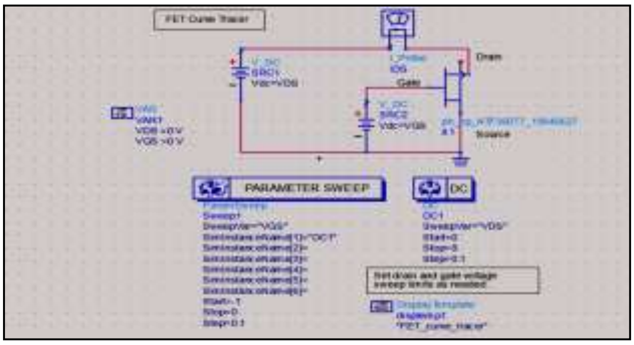

Figure. 3. Schematic set up for curve tracer

The simulation result of curve tracer is shown in figure 4:

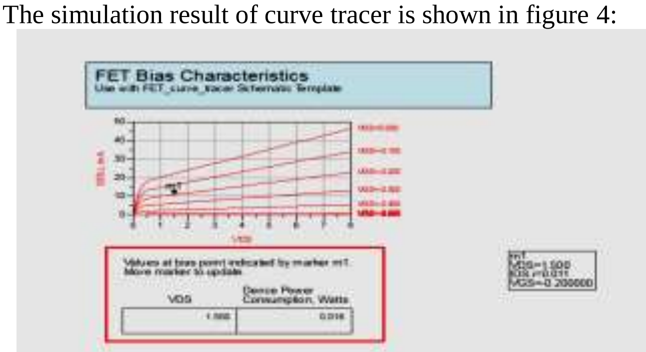

Figure 4. FET curve tracer output

Marker m1 in the figure 4 of curve tracer graph shows the point which is chosen for biasing the transistor to operate in class E. The schematic of parallel circuit class E amplifier built with lumped components.

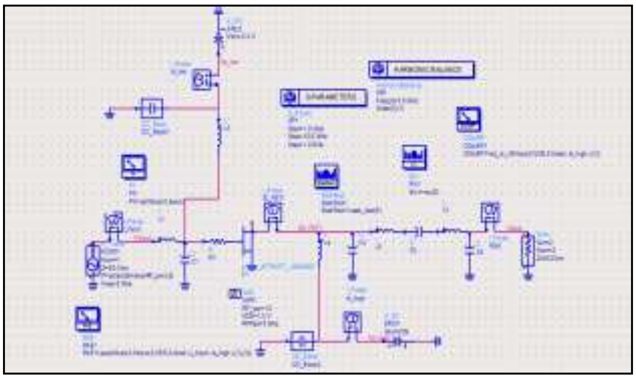

Figure 5. Schematic of single stage class E amplifier

Class E amplifier is designed in ADS2011 tool the load network values are calculated using standard design equations. The amplifier is simulated, the plots of current and voltage waveform across the transistor is shown below:

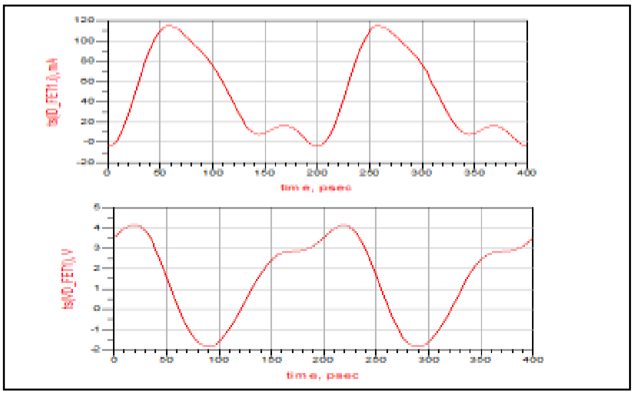

Figure 6: Current and voltage output at transistor

Above result shows the current and voltage waveforms are 180° out of phase to each other thus minimizing power dissipation in circuit.

Harmonic balance simulation is performed on the amplifier to obtain the output power, power added efficiency, drain efficiency.

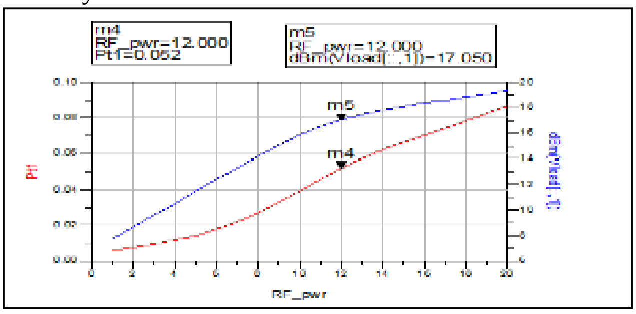

Figure 7: Output voltage and output power of the parallel circuit class E amplifier

The power of 0.052Watts and voltage of 17.050 dBm are obtained at the load are shown in figure 7.

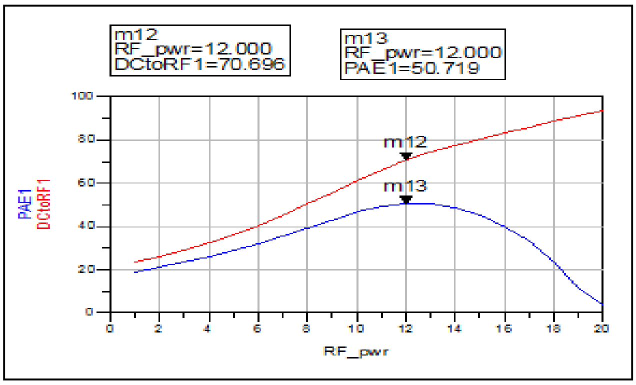

Figure 8: Drain efficiency and power added efficiency output of single stage parallel circuit class E amplifier

PAE of 50.719% and η of 70.696% is obtained for single stage amplifier is plotted in figure8.

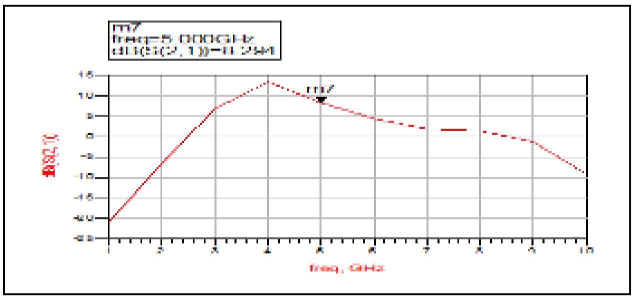

Figure 9: Gain of Class E amplifier

Gain of 8.294 dB is obtained for single stage parallel circuit class E amplifier

Schematic below shows the simulation set up to perform two tone analysis for single stage parallel circuit class E amplifier

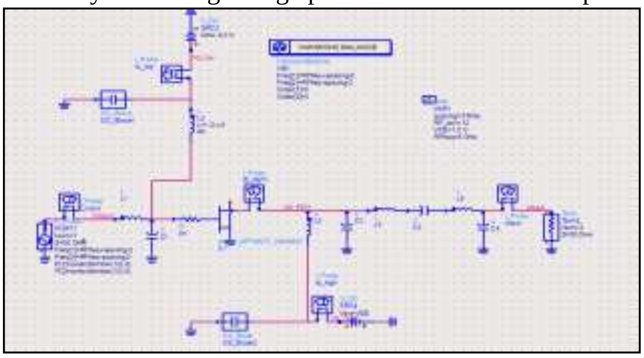

Figure 10: Schematic of two tone test

The Simulated results below shows the third order intermodulation frequency.

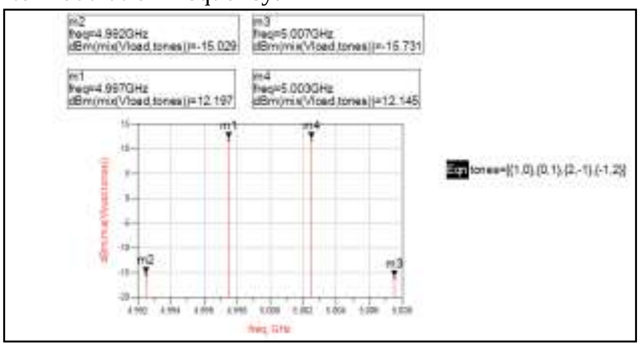

Figure11. Two tone analysis output of single stage parallel circuit class E amplifier

Schematic for 1dB gain compression point simulation

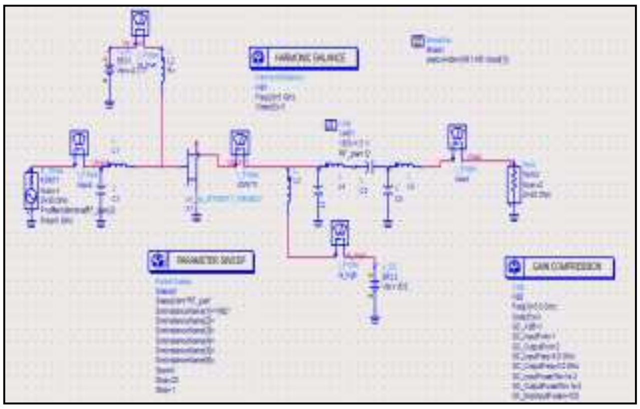

Figure12. Schematic to obtain 1 dB gain compression point

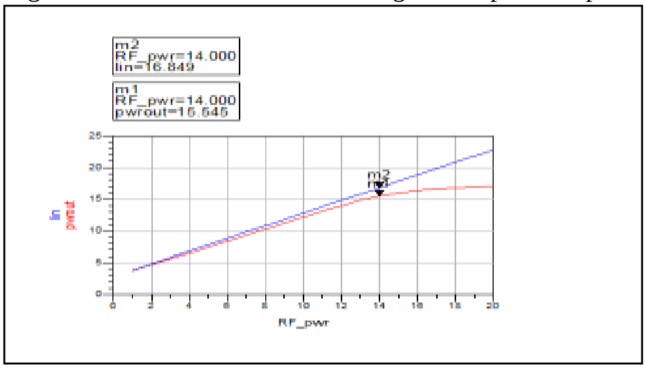

Figure13. Simulated result of 1 dB gain compression point

From the above graph it can be seen amplifier output starts deviating from linear output at radio frequency (RF) input 12 dBm. The schematic of two stage parallel circuit class E amplifier to perform harmonic balance and s-parameter simulation is shown in figure 14 below:

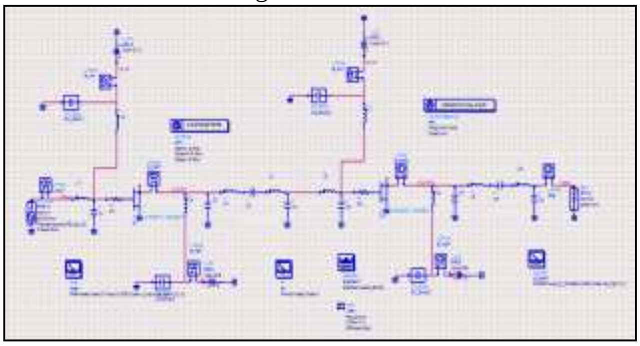

Figure. 14. Schematic of 2 stage parallel circuit class E amplifier

The simulated output for current and voltage waveforms of two stage class E amplifier are shown below

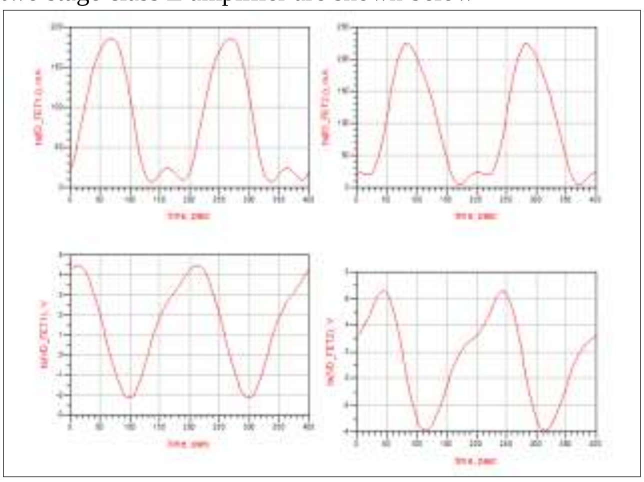

Figure. 15. Simulated results of current and voltage waveform of 2 stage parallel circuit class E amplifier

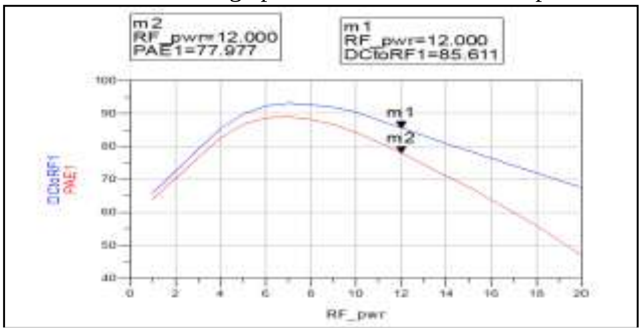

Figure 16: Simulated values of power added efficiency and drain efficiency

Power added efficiency of 77.977% and drain efficiency of 85.611% are obtained for two stage parallel circuit class E amplifiers is plotted below:

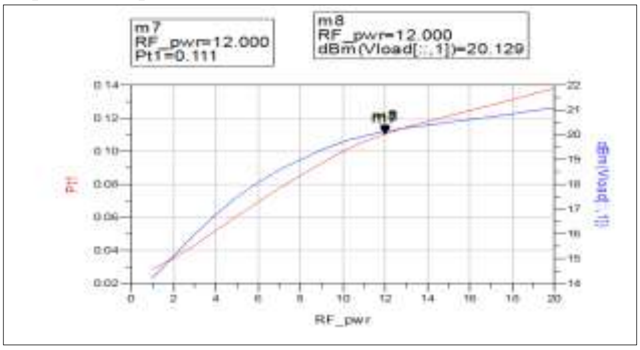

Figure 17: power and voltage obtained at output of two stage parallel circuit class E amplifier

The output power of 0.111W and output voltage of 20.129 dBm is obtained for two stage parallel circuit class E amplifier.

Figure18: Gain of 2 stage parallel circuit class E amplifier

Gain obtained at the output of two stage class E amplifier is 16.036 dB.

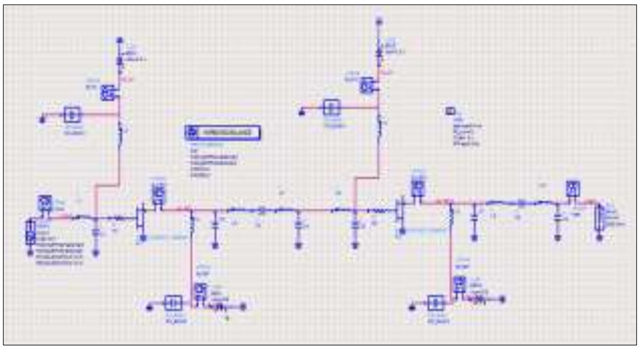

Figure 19: Schematic of two stage parallel circuit class E amplifier for two tone test

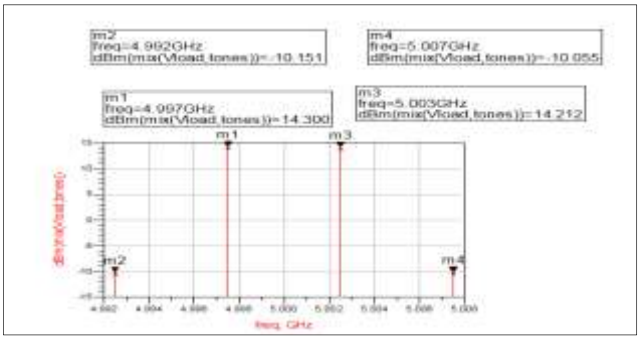

Figure.20: Output power spectrum obtained for two test simulation

Power output at third intermodulation frequency is -10 dBm the difference between the fundamental and third harmonic frequency is around 24dBc.

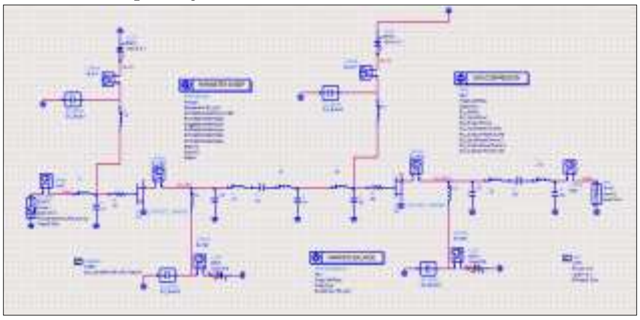

Figure.21: Schematic of two stage Class E amplifier for gain compression simulation

Figure.22. 1 dB gain compression of 2 stage class E amplifier

The figure 22, shows the 1 dB gain compression of two stage class E amplifier. The output power starts deviating at 12 dBm of input RF power.

VI.CONCLUSION

The parallel circuit class E amplifier is designed and simulated in ADS tool, the results shows better power added efficiency and drain efficiency at 5GHz. Transistor used to design both the single and two stage amplifiers is GaAs p-HEMT. The load network elements are tuned to achieve current and voltage at the drain of transistor to be 180^{o} out of phase as a result power dissipation is minimized and efficiency is increased.

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