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Simulation & Analysis of 3ϕ (5&7 level) Diode Clamped Multilevel inverter fed to Induction Motor

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Abstract: *Use of multilevel inverters has become popular in recent years for high power applications and an effective and practical solution for increasing power and reducing harmonics of AC waveforms. By synthesizing the AC output voltage from several levels of DC voltages, stair case output waveform can be produced. This allows for high output voltage and simultaneously lowers the stress on the semiconductor device, complexity of control and introduce voltage unbalancing problems. In this paper the proposed topology requires less number of switches, free from voltage unbalancing problems and reduced complexity when compared to other topology of available multilevel inverters Neutral Point Clamped and Flying Capacitor. This topology shown the requirement of components and compared to other topologies to show the superiority. The simulation results of proposed topology three phase five-level and seven-level multilevel inverter fed induction motor drive are verified using MATLAB. The THD between five-level and seven-level inverter is compared it can be observed that in the higher levels THD is reduced.*

Keywords: Diode Clamped Multilevel Inverter (DCMI); Induction Motor (IM), SPWM technique, Total Harmonics Distortion (THD).

1. Introduction

The first invention in multilevel converters was the so-called neutral point clamped inverter. A three-phase diode clamped multilevel inverter fed induction motor is described. The diode clamped inverter provides multiple voltage levels from a five level unidirectional voltage balancing method of diode clamped inverter [1]. The voltage across the switches has only half of the dc bus voltage. These features effectively double the power rating of voltage source inverter for a given semiconductor device [2]. The proposed inverter can reduce the harmonic contents by using multicarrier SPWM technique. It generates motor currents of high quality, reduced losses and increases efficiency of induction motor.

For research on multi-level inverter topologies, a preferred multilevel inverter topology shall have the following characteristics:

1) The level is easy to extend.
2) When the number of levels is high enough, the harmonic content is low.
3) There is no need for filters.
4) Inverter efficiency is high because all devices are switched at the fundamental frequency.
5) The control method is simple.

Performance of multilevel inverters depends on the PWM converter topology. In two-level or multilevel inverters, there is only one turn-on, turn-off per device per cycle. With these converters, the ac output voltage can be controlled, by varying the width of the voltage pulses, and/or the amplitude of the dc bus voltage. Another approach is to have multiple pulses per half-cycle, and then vary the width of the pulses to vary the amplitude of the ac voltage. The principle reason for doing so is to be able to vary the ac output voltage and to reduce the low-order harmonics. PWM switching strategies not only addresses the primary issues viz, less THD. Among various modulation techniques [3] for a multilevel inverter, sin-triangle pulse width modulation (SPWM) is an attractive candidate due to the following merits. It proportionally varies the width of each pulse to the amplitude of a sine wave evaluated at the center of the same pulse [4]. It is suitable for MATLAB/SIMULINK implementation.

In sin-triangle PWM, three phase reference modulating signals are compared against a common triangular carrier to generate PWM pulses for the three phases. Reduction of total harmonics distortion (THD) of inverter output voltage and the distortion seamless when level of diode-clamped inverter has got increased is the main advantage of the proposed control method.

Generally there are following types of multilevel inverter
1] Multilevel inverter using IGBT/MOSFET/GTO.
2] Multilevel inverter using thyristor

2. Diode Clamp Multilevel Inverter (DCMI)

a) Five Level Diode Clamp Multilevel Inverter

An *m*-level diode-clamped multilevel inverter typically consists of *m* –1 capacitors on the dc bus and produces *m* levels of the phase voltage [5]. A three-phase five-level structure of a DCMLI is shown in Figure.1. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by four capacitors into five levels. The voltage across each capacitor is V_{dc}, and the voltage stress across each switching device is limited to V_{dc} through the clamping diodes.

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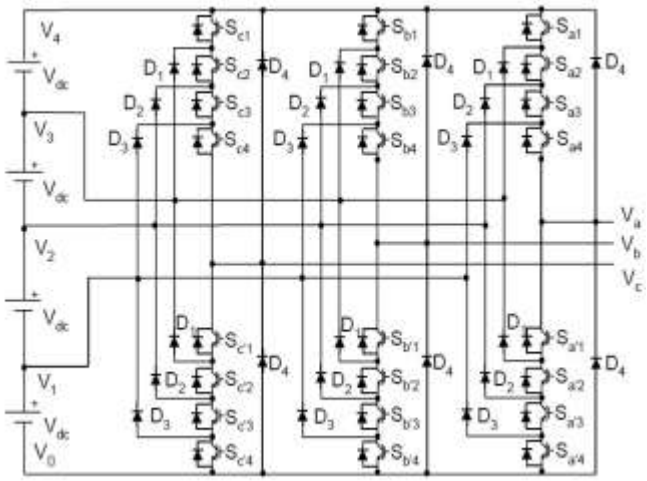

Figure 1: A three phase five level DCMI schematic

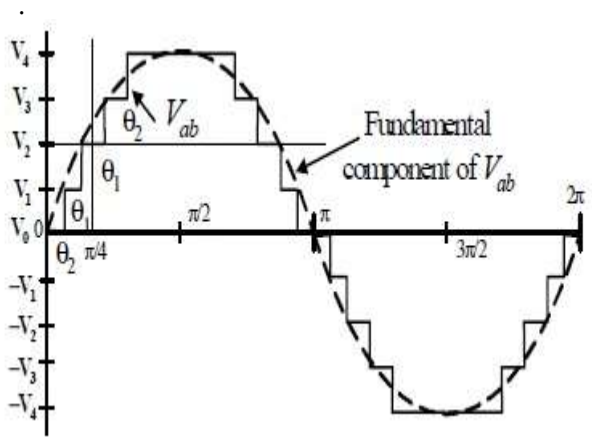

Figure 2: Staircase line voltage waveform of five levels DCMI

The figure 2: Show staircase line voltage waveform of five levels DCMI of one leg.

b) Seven Level Diode clamp multilevel Inverter

The seven-level diode clamped multilevel Inverter is shown in Figure.3. It contains 36 unidirectional active switches and 36 neutral point clamping diodes. The middle point of the 6 capacitors "*n"* can be defined as the neutral point [6]. The major benefit of this configuration is each switch must block only one-half of the dc link voltage (V_{dc}/6). In order to produce seven levels, only two of the twelve switches in each phase leg should be turned on at any time. The dc-bus voltage is split into three levels by two series-connected bulk capacitors, C1, C2, C3, C4, C5 and C, 6. They are same in rating. The diodes are all same type to provide equal voltage sharing and to clamp the same voltage level across the switch, when the switch is in off condition. Hence this structure provides less voltage stress across the switch.

An *m*-level diode-clamped multilevel inverter typically consists of *m* –1 capacitors on the dc bus and produces *m* levels of the phase voltage [7]. A three-phase seven-level structure of a DCMLI is shown in Figure: 3. each of the three phases of the inverter shares a common dc bus, which has been subdivided by six capacitors into seven levels. The voltage across each capacitor is V_{dc}/6, and the voltage stress across each switching device is limited to V_{dc} /6 through the clamping diodes.

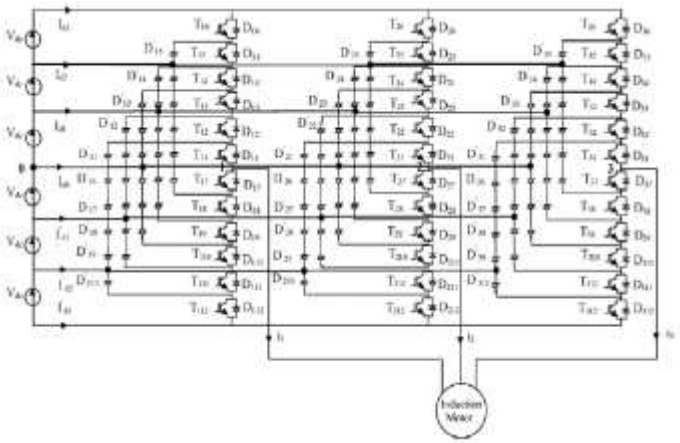

Figure 3: A three phase seven level DCMI schematic

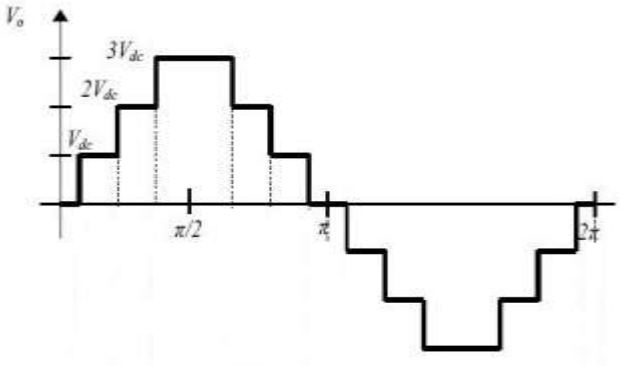

Figure 4: Staircase line voltage waveform of seven levels DCMI

The figure.4: Show staircase line voltage waveform of seven levels DCMI of one leg.

3. SPWM METHOD

This Paper mainly focuses on multicarrier SPWM method. This method is simple and more flexible than SVM methods. The multicarrier SPWM method uses several triangular carrier signals, keeping only one modulating sinusoidal signal. If an n-level inverter is employed, n-1 carriers will be needed. The carriers have the same frequency WC and the same peak to peak amplitude Ac and are disposed so that the bands they occupy are contiguous. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency W_m and amplitude Am. At every instant each carrier is compared with the modulating signal [8]. Each comparison gives 1(-1) if the modulating signal is greater than (lower than) the triangular carrier in the first (second) half of the fundamental period, 0 otherwise. The results are added to give the voltage level, which is required at the output terminal of the inverter.

Multicarrier PWM method can be categorized into Two groups:

1) Carrier Disposition (CD) method
2) Phase shifted PWM method.

Advantages of multicarrier SPWM techniques

- Easily extensible to high number of levels.
- Easy to implement.
- To distribute the switching signals correctly in order to minimize the switching losses.
- To compensate unbalanced dc sources.

- With this method, lower order harmonics can be eliminated or minimized Along with its output voltage control.
- As higher order harmonics can be filtered easily the higher order harmonics can be minimized [9].

4. Simulation of Diode Clamped Multilevel Inverter:

a) Operation of 5 Level Diode Clamped Multilevel Inverter:

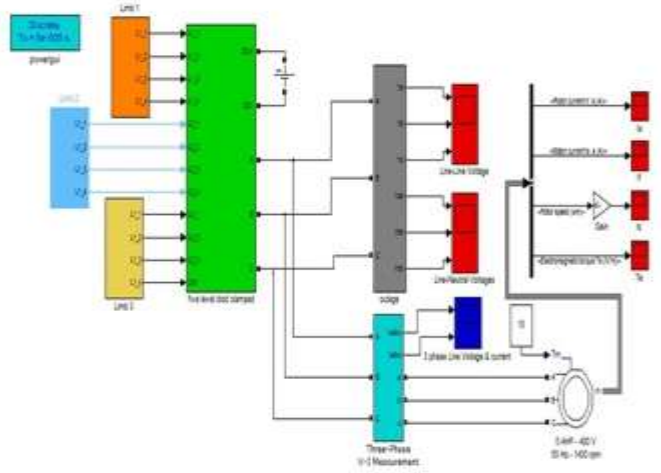

Figure 4: Simulink diagram of 5-level multilevel inverter for Induction Motor drive

To produce a staircase-output voltage, consider 3Φ five-level diode clamped multilevel inverter as shown in Figure. 4. The steps to synthesize the five-level voltages are as follows.

- For an output voltage level $V_{ao}=V_{dc}$, turn on all upper-half switches $S_1.S_2.S_3.S_4$ and turn off all lower-half switches $S_1'.S_2'.S_3'.S_4'$.
- For an output voltage level $V_{ao}=3V_{dc}/4$, turn on all upper-half switches $S_2.S_3.S_4$ and lower-half switch S_1'.
- For an output voltage level $V_{ao}=V_{dc}/2$, turn on all lower half switches $S_3.S4$ and lower-half switches $S_1'.S_2'$.
- For an output voltage level $V_{ao}=V_{dc}/4$, turn on all lower half switch S_4 and lower-half switches $S_1'.S_2'.S_3'$.
- For an output voltage level $V_{ao}=0$, turn off all upper-half switches $S_1.S_2.S_3.S_4$ and turn on of all lower-half switches $S_1'.S_2'.S_3'.S_4'$ [10].

Table 1: Switching states for 5-level inverter

Output Va0	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3= V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2= V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

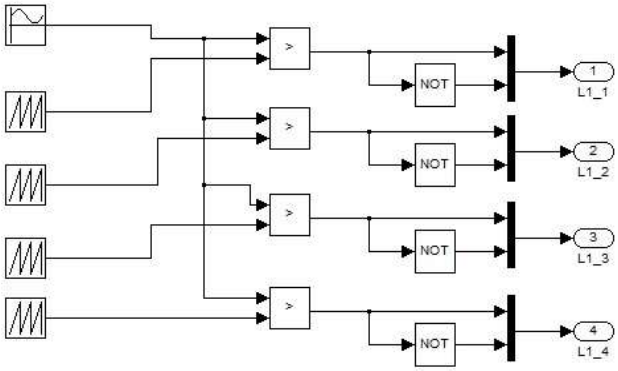

Figure 5: Pulse generation circuit of 5 levels DCMI

a) Operation of 7 Level Diode Clamped Multilevel inverter:

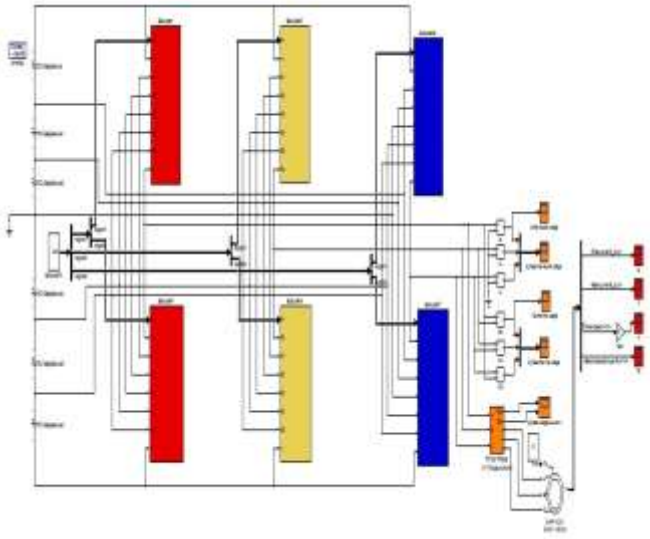

Figure 6: Simulink diagram of Seven-level multilevel inverter for Induction motor drive

To produce a staircase-output voltage, consider three leg of the three-level inverter, as shown in Figure. 6. The steps to synthesize the seven-level voltages are as follows.

- For an output voltage level $V_{ao}=V_{dc}$, turn on all upper-half switches $S_1.S_2.S_3.S_4.S_5.S_6$ and turn off all lower-half switches $S_1'.S_2'.S_3'.S_4'.S_5'.S_6'$.
- For an output voltage level $V_{ao}=4V_{dc}/6$, turn on upper-half switches $S_2.S_3.S_4.S_5.S_6$ and one lower switches S_1'.
- For an output voltage level $V_{ao}=5V_{dc}/6$, turn on upper-half switches $S_3.S_4.S_5.S_6$ and lower-half switches $S_1'.S_2'$.
- For an output voltage level $V_{ao}=V_{dc}/2$, turn on upper-half switches $S_4.S_5.S_6$ and lower-half switches $S_1'.S_2'.S_3'$.
- For an output voltage level $V_{ao}=V_{dc}/3$, turn on upper-half switches $S_5.S_6$ and lower-half switches $S_1'.S_2'.S_3'.S_4'$.
- For an output voltage level $V_{ao}=V_{dc}/6$, turn on upper-half switch S_6 and lower-half switches $S_1'.S_2'.S_3'.S_4'.S_5'$.
- For an output voltage level $V_{ao}=0$, turn off all upper-half switches $S_1.S_2.S_3.S_4.S_5.S_6$ and turn on all lower-half switches $S_1'.S_2'.S_3'.S_4'.S_5'.S_6'$ [11].

Table 2: Switching states for 5-level inverter

Output Vab	S_1	S_2	S_3	S_4	S_5	S_6	S_1'	S_2'	S_3'	S_4'	S_5'	S_6'
$V_7=V_{dc}$	1	1	1	1	1	1	0	0	0	0	0	0
$V_6=5V_{dc}/6$	0	1	1	1	1	0	1	0	0	0	0	0
$V_5=4V_{dc}/6$	0	0	1	1	1	1	1	1	0	0	0	0
$V_4=V_{dc}/2$	0	0	0	1	1	1	1	1	1	0	0	0
$V_3=V_{dc}/3$	0	0	0	0	1	1	1	1	1	1	0	0
$V_2=V_{dc}/6$	0	0	0	0	0	1	1	1	1	1	1	0
$V_1=0$	0	0	0	0	0	0	1	1	1	1	1	1

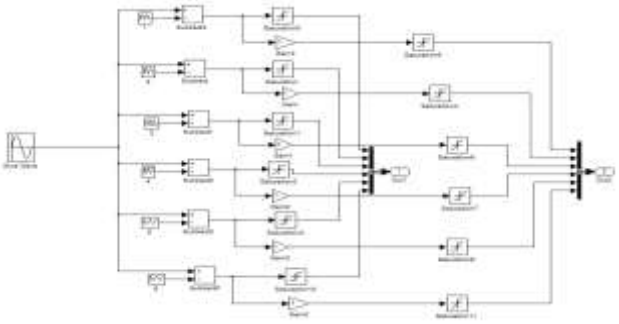

Figure 6: Pulse generation circuit of 7 levels DCMI

5. Simulation Results:

a) Simulation Results of 5 Level Diode Clamped Multilevel Inverter:

The performance of three phase induction motor five-level inverter is shown in figure: 7. The Line voltage is shown in fig.7 (a). The seven-level line to neutral voltage is shown in fig.7 (b). The fig.7(c), (d), (e), (f) are 3Φ line voltage, current, stator & rotor current. The fig.7 (g), (h) is the Induction motor speed in R.P.M and Electromagnetic Torque in Newton meter respectively.

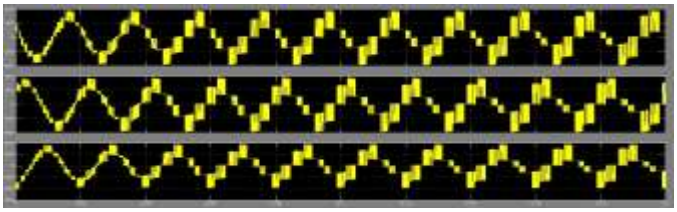

Figure: 7(a): Line to line voltage waveform of 5 levels DCMI

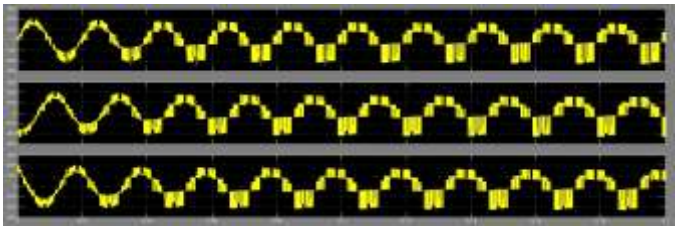

Figure 7(b): Line to neutral voltage waveform of 5 levels DCMI

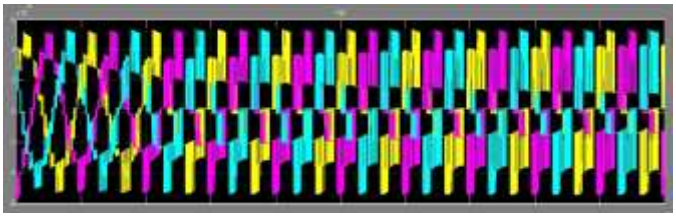

Figure 7(c): Three phase line voltage waveform of 5 levels DCMI

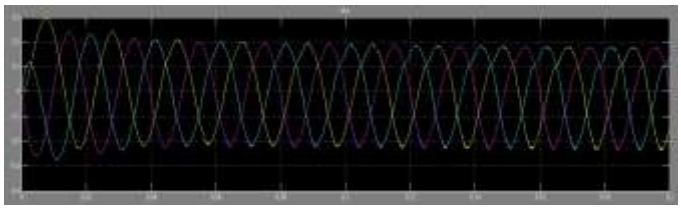

Figure 7(d): Three phase current waveform of 5 levels DCMI

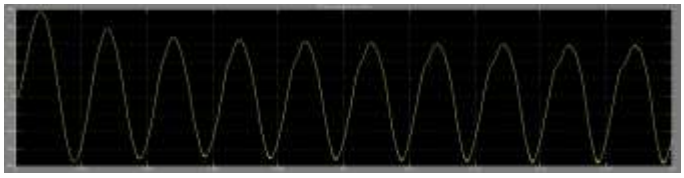

Figure 7(e): Stator current waveform of 5 levels DCMI

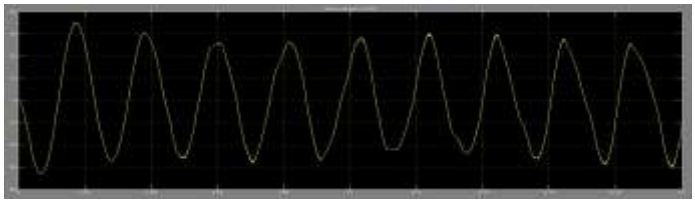

Figure 7(f): Rotor current waveform of 5 levels DCMI

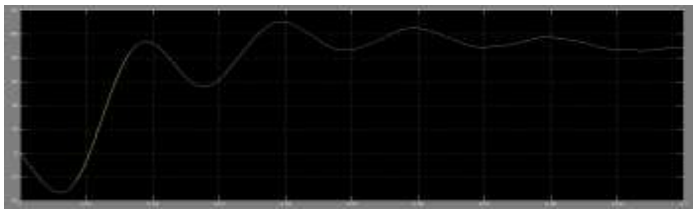

Figure 7(g): Speed waveform of 5 levels DCMI

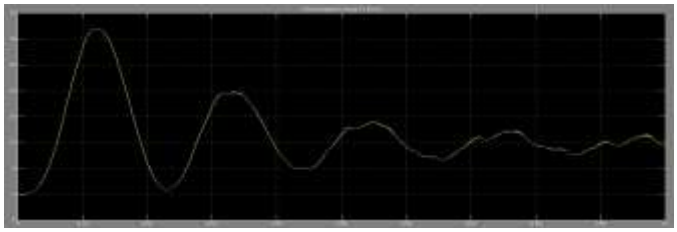

Figure 7(h): Torque waveform of 5 levels DCMI

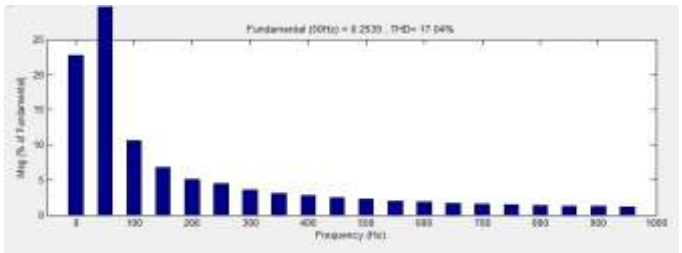

Figure 7(i): THD waveform of 5 levels DCMI

b) Simulation Results of 7 Level Diode Clamped Multilevel Inverter:

The performance of three phase induction motor seven-level inverter is shown in figure: 8. The Line voltage is shown in fig.8 (a). The seven-level line to neutral voltage is shown in fig.8 (b). The fig.8(c), (d), (e), (f) are 3Φ line

voltage, current, stator & rotor current. The fig.8 (g), (h) is the Induction motor speed in R.P.M and Electromagnetic Torque in Newton meter respectively.

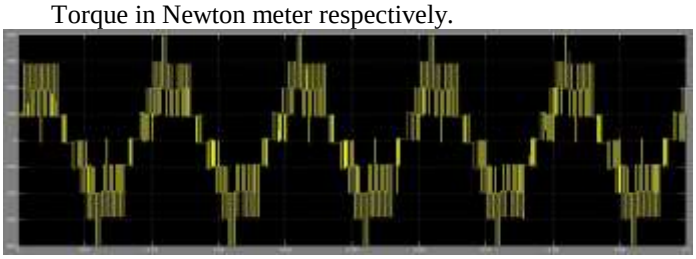

Figure 8(a): Line to line voltage waveform of 7 levels DCMI

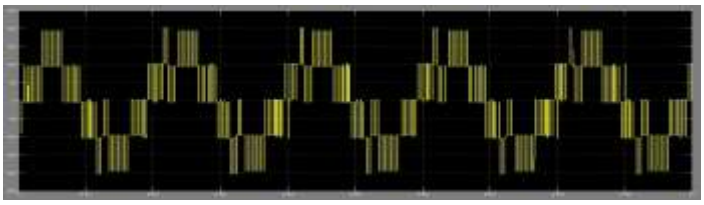

Figure 8(b): Line to neutral voltage waveform of 7 levels DCMI

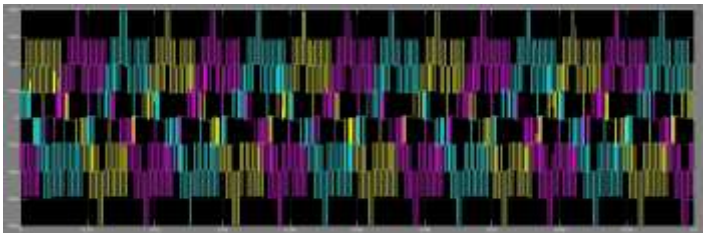

Figure 8(c): Three phase line voltage waveform of 7 levels DCMI

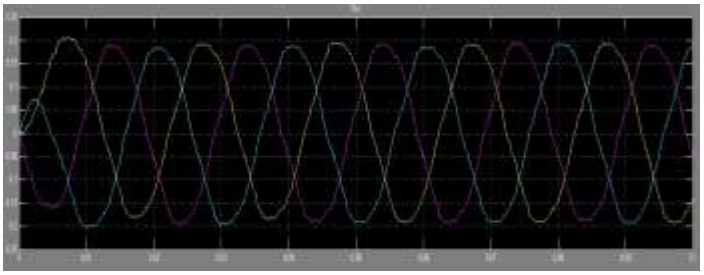

Figure 8(d): Three phase current waveform of 7 levels DCMI

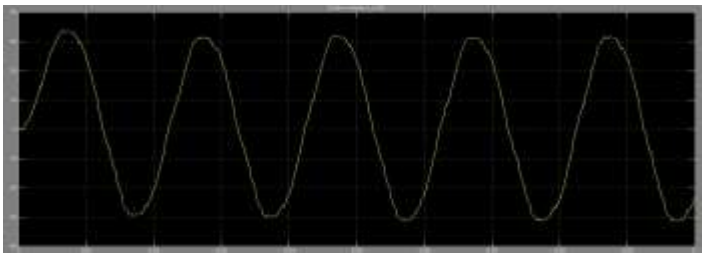

Figure 8(e): Stator current waveform of 7 levels DCMI

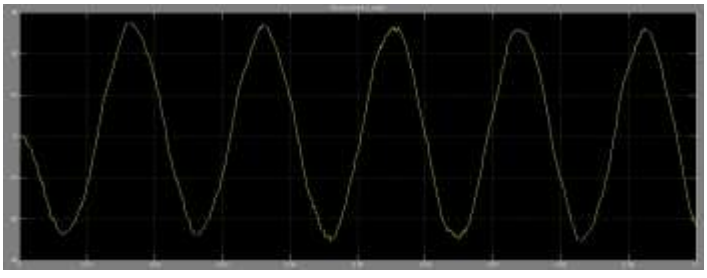

Figure 8(f): Rotor current waveform of 7 levels DCMI

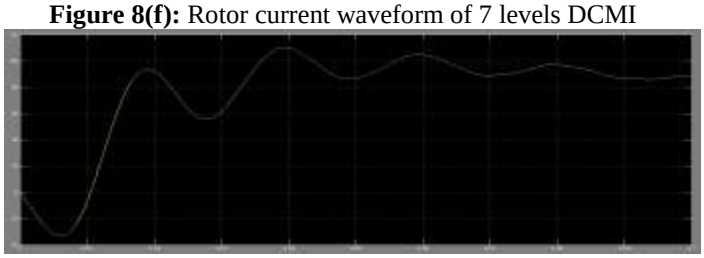

Figure 8(g): Speed waveform of 7 levels DCMI

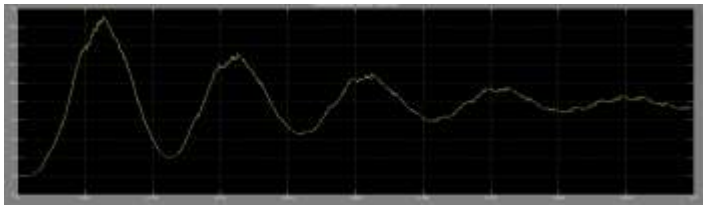

Figure 8(h): Torque waveform of 7 levels DCMI

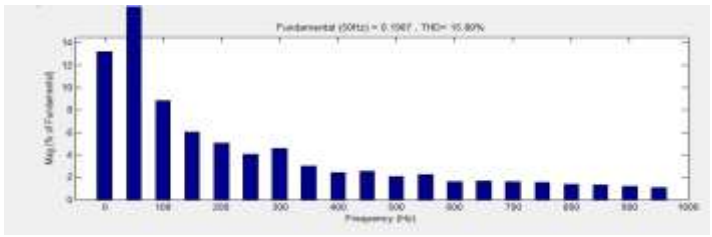

Figure 8(i): THD waveform of 7 levels DCMI

6. THD Comparison:

Table 3: Comparison 5 & 7 Level THD of DCMI

Sr. No	Level	Fundamental component of frequency (50Hz)	% THD (Total Harmonics Distortion)
1	Five	0.2529	17.04
2	Seven	0.1907	15.80

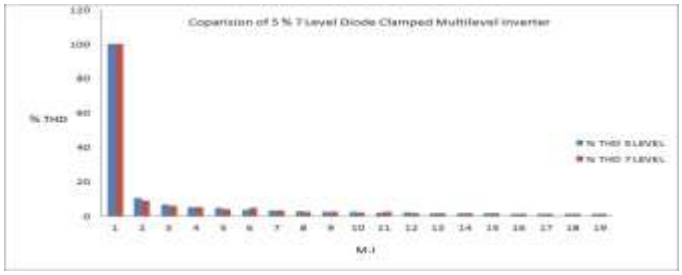

Figure 9: THD vs. MI of five and seven-level inverter

The comparison between the THD of both 3ϕ 5 and 7-level inverter with respect to Modulation index is shown in fig.9. It can be observed that in the higher levels the THD of the multilevel inverter is reduced.

Table 4: Modulation Index Vs THD

Frequency	M.I	% THD 5 LEVEL	% THD 7 LEVEL
50	0	100	100
100	1	10.57	8.83
150	2	6.75	6.02
200	3	5.06	5.02
250	4	4.52	4.06
300	5	3.52	4.59
350	6	3.05	3.01
400	7	2.77	2.39
450	8	2.43	2.53
500	9	2.29	2.07
550	10	1.96	2.26
600	11	1.82	1.59
650	12	1.69	1.67
700	13	1.59	1.63
750	14	1.46	1.54
800	15	1.33	1.39
850	16	1.28	1.29
900	17	1.22	1.22
950	18	1.2	1.05

7. Conclusions:

In this paper, a new multilevel topology in five-level and seven-level inverter fed induction motor drive is implemented. In seven-level inverter circuit modified diode clamped inverter is used for reducing the switching devices and higher reliability. Here SPWM controller has less complexity when compared to five level inverter.

The THD is compared of five-level and seven-level inverters. It can be observed that in the higher levels THD is reduced. The simulation results of proposed topology of three phase five level and seven level diode clamped multilevel inverter fed induction motor drive are verified using MATLAB.

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