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A Novel Energy Efficient Transmission gate Voltage Level Shifter for multi VDD systems

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Abstract: *A new design of level-up and level-down shifter for low-power and high speed applications has been presented. Level-up and level-down operations can be perform by using the new well-organized Transmission gate Voltage Level Shifter (TVLS). In this paper a novel voltage level shifter have introduced that performs level-up shift or level-down shifts. In this, the circuit watch its input logic voltages and perform leve-up shift, when its input voltage is low and level-down shift when its input voltage is high. This TVLS constantly performs level-up shift from 0.4V to 1V and level-down shift from 1V to 0.4V. The schematic design has been design and simulated using 90nm CMOS process technology. In analysis of power and delay, TVLS has level-up and level-down average power consumption is 24.7145nW and with a propagation delay of 2.053ns has obtained at 1 MHz.*

Keywords: up shift, down shift, Voltage Level shifter, power, delay**.**

1. Introduction

The major concern in VLSI design is area, performance, cost and consistency. Consideration of power was mostly given the secondary importance. In recent years, however, this has begun to change and gradually, power is given importance to area and speed specifications. Many factors have given an idea to this trend. In the past, the device concentration and operating frequency were low enough that it was not a constraining cause in the chips. With the wide applications of battery supplying devices, such as portable PC, cellar phones and PDA, power consumption has become a critical design concern in today's VLSI circuit and system designs. Additionally, approximately millions of transistors have been packed into a single chip in nanometer technologies. As the scale of integration develops, several transistors, quicker and lesser than their previous designs, are being crowded into a single chip [1]. This contributes to the steady growth of the operating frequency and processing capacity per chip, which increases power dissipation. This huge power consumption leads to the heat dissipation that can adversely affect reliability and designing packaging cost. These constraints gave much importance to low power design of CMOS circuits and driven numerous research efforts to address various kinds of power reduction techniques.

When technology scales down, total power dissipation will decrease and at the same time delay varies depends upon supply voltage, threshold voltage, width to length ratio, thickness of oxide, load capacitance. CMOS devices have bought a drastic change in each technology generation to achieve higher integration density and performance. Hence increase in leakage current aggressively with technology scaling and become a major contributor to the total IC power.

The multiple supply system provides a high-voltage supply for high-performance circuits and a low-voltage supply for low-performance circuits. In a dual VDD circuit, the reduced voltage (Low VDD) is applied to the circuit on non-critical paths, while the original voltage (High VDD) is applied to the circuit on critical paths. Since the critical path of the circuit is unchanged, this transformation preserves the circuit performance. If a gate supplied with VDDL drives a gate supplied with VDDH, the pMOS may never turn off. Therefore a level shifter is required whenever a module at the lower supply drives a gate at the higher supply. Level converters are not needed for a step-down change in voltage [2], [9]. The transition from low to high V_{dd} is condensed into the level shifters shown in the figure. In other words, In recent VLSI circuits and system designs the applications of handheld gadgets are becoming more, power consumption has grown to be a discriminating configuration concern. Now a days, more or less millions of transistors have been crowded into a single chip using nanometer technologies. Voltage islands, operating at different voltages means the two or more supply voltages can be maintained among multi cores or multi functional blocks or even dividing a single chip by isolating the integrated circuit into regions. The circuits that are on the discriminating path are influenced with higher VDD and the circuits which are off the discriminating path are influenced with lower VDD to decrease the power consumption, in additional high speed perceptive paths are controlled with higher VDD and low speed perceptive paths can be controlled with lower VDD because power consumption is directly proportional to the square of the supply voltage [3], [10], [11]. A Level Shifter is required to interface both VDDH and VDDL circuits (two or more supply VDD systems). A level shifter which is placed between two or more VDD systems is important to keep away from the current that may lead to unwanted power consumption. In short, a level shifter is a effortless circuit that shifts the input voltage from one voltage level to another voltage level without any static power consumption.

Fig 1 clearly gives an idea of level shifter, which shows a two or more VDD system where the entire system is separated into modules. Modules means, it can be a many cores or functional blocks or voltage islands, working with dissimilar supply voltages.

In various electronic applications, level shifters are the core elements that are used to shift the logic signal from one voltage level to other voltage level. In view of literature, level shifter can be mainly categorized into two types:

Level up shifter and Level down shifter. A higher voltage level (VDDH) is obtained from the input voltage (VDDL) in level up shifter. On the other hand a lower voltage level (VDDL) is obtained from the input voltage (VDDH) in level down shifter. As a result a Level shifter (LS) can perform voltage level up shift from 1.8V to 2.5V and voltage level down shift from 2.5V to 1.8V.

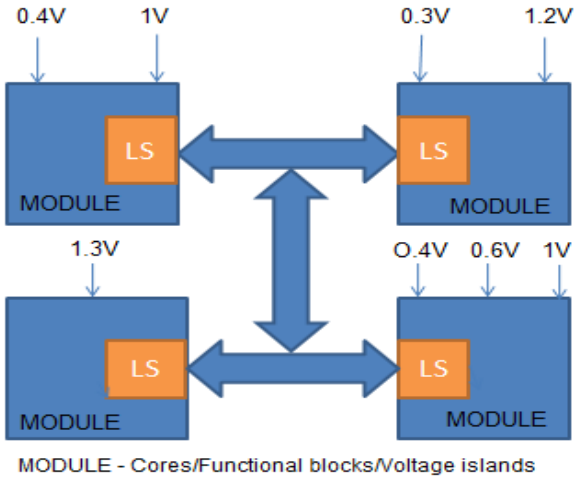

Figure 1: Level shifter basic block diagram.

2. Existing Level Shifters

The basic and fundamental level shifter configuration is the Differential Cascade Voltage Switch (DCVS) circuit, can be viewed in the Figure 2. It is a just half latch type, constructed by two PMOSFETs MP2 and MP3 & two NMOSFETs MN2 and MN3, and these devices are driving by the level shifting input voltage (VIN) and its complement.

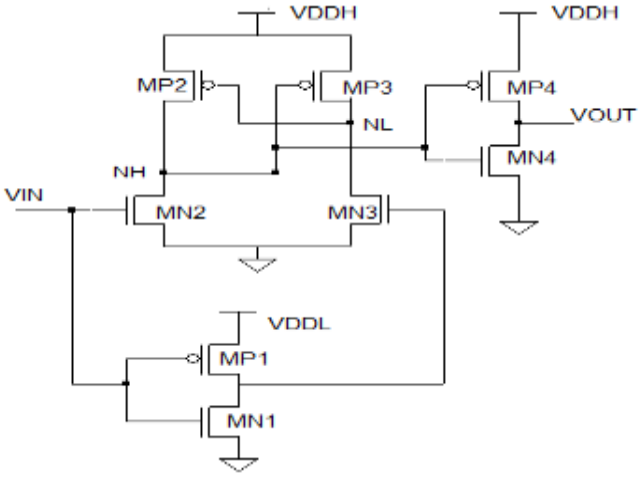

Figure 2: Conventional DCVSL level shifter

While the input VIN transition from low to high, the MN2 will becomes ON and MN3 becomes OFF, As a result, the node voltages at NH and NL are pulled down and pulled up respectively, leading to MP3 becomes ON and MP2 becomes OFF. When MP3 becomes on, the voltage at NL will become equal to VDDH and MP2 will become turned OFF, and the voltage at NH stats to be discharged. There may be impedance issue between the devices. Thus draw up system qualities and force down system qualities ought to be decisively adjusted to keep up the obliged rationale levels. It is monotonous undertaking to attain to when the level moving signs are at sub limit voltage level [4], [12].

The Level Shifter design proposed by Shien-Chun Luo et al. [5] has designed modified level shifter for the reduction of the dynamic power by modifying widths and lengths of the MOS transistors. It may reduce dynamic power, but poor performance may results in leakage power and delay.

3. PROPOSED LEVEL SHIFTER

3.1 Transmission gate Voltage Level Shifter

The proposed level shifter model performs both up movement and down movement in light of its input voltage. The circuit diagram of TVLS is indicated in Fig 3. Here two voltage sources are utilized i.e., VDDH and VDDL. In view of the connected voltages both of the voltage sources is chosen based on input voltage. For up movement VDDH is chosen and for down movement VDDL is chosen by the data input voltage called VIN, So the resultant voltage level will be VDDH or VDDL or 0V.

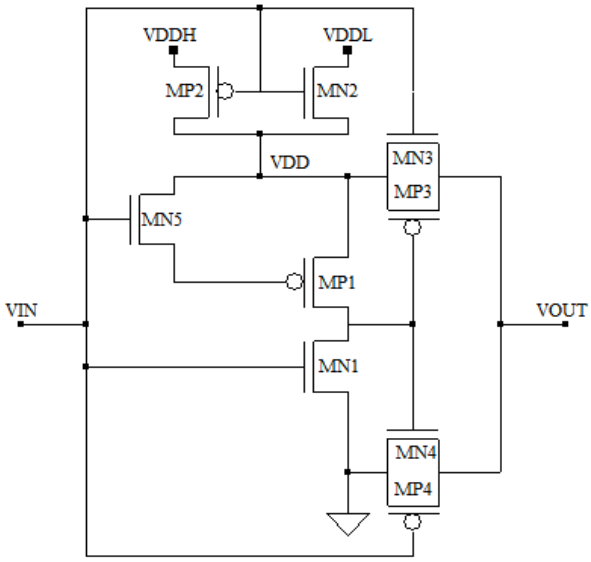

Figure 3: Proposed TVLS

3.2 TVLS circuit operation

The proposed design in Fig 3, Consists of mainly two parts they are:

The MOSFETs MP2 and MN2 acts as 2X1 Multiplexer, either of supply voltages VDDH or VDDL can selected based on the input voltage VIN. Then VIN can be considered as select line.

The rest of the circuit performs level shifting operation. The upper transmission gate comprising with MN3 and MP3 useful to make VOUT equals to VDDH or VDDL and the lower transmission gate comprising with MN4 and MP4 useful to make VOUT equals to VSS.

To perform circuit analysis, the VDDH is taken 1V and VDDL is 0.4V. When VIN is at 0.4V, the MP2, MN1 and MN5 will turn ON and MP1 will turns OFF. So VDD becomes VDDH, at the same time upper transmission gate also turn ON, hence VDDH will appears at VOUT. Thus VOUT will be charged to VDDH i.e. 1V, Level-up is the resultant. When VIN is at 1V, the MN3, MN1 and MN5 will turn ON and MP1 will turns OFF. So VDD becomes VDDL, at the same time upper transmission gate also turn ON, hence VDDL will appears at VOUT. Thus VOUT will be charged to VDDH i.e. 0.4V, level-down is the resultant.

When VIN is at 0V, the MN2, MN1 and MN5 will turn OFF and MP2 and MP1 will turns ON. So VDD becomes VDDH, at the same time lower transmission gate also turn ON, hence VOUT will be discharged to VSS i.e. 0V.

4. Simulation Results And Discussions

The circuit is outlined and simulated in HSPICE utilizing 90nm technology. The threshold voltages (V_{TH}) of PMOS are -0.3V and NMOS are 0.3V maintained.

4.1 Waveforms

The simulated wave structures demonstrated in the Fig 4 and 5 are the level up and level shifts at the frequency of 1MHz. In Fig 4 when data is at 0.4V yield is 1V (Up shift). In Fig 5 when data is at 1V yield is 0.4V (Down shift).

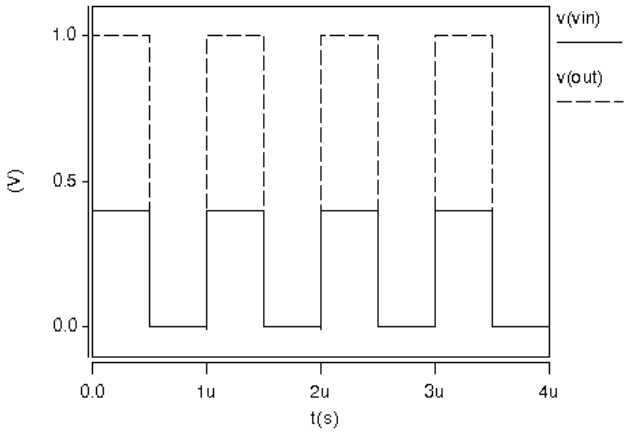

Figure 4: Waveform of Level up shift

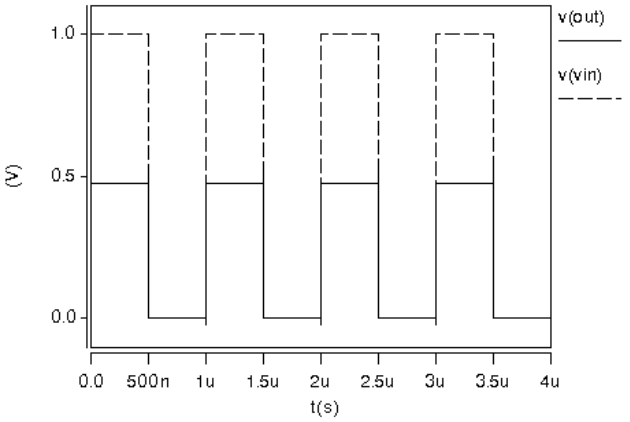

Figure 5: Waveform of Level down shift

4.2 Performance analysis

The performance examination of the proposed TVLS is indicated in the Table I. It demonstrates the normal power utilization, delay of the proposed TVLS for performing level up shift and down shift. The normal power utilization is 29.83nW for up movement and 19.59nW for down movement as shown in the fig. 6 as a function of VIN. Propagation Delay between input and output is 1.229nS for up movement and 2.87nS for down movement.

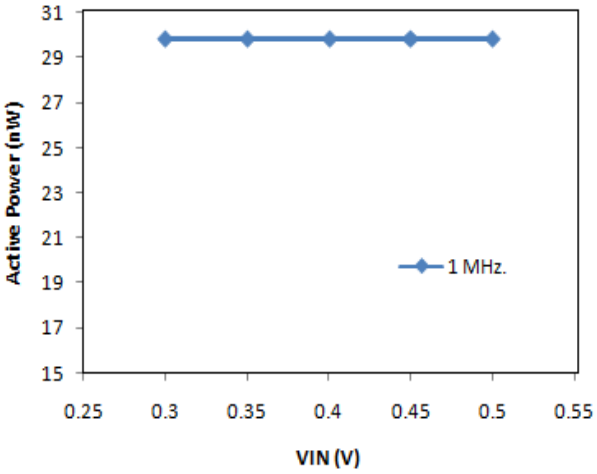

Figure 6 (a): At constant VDDH=1V

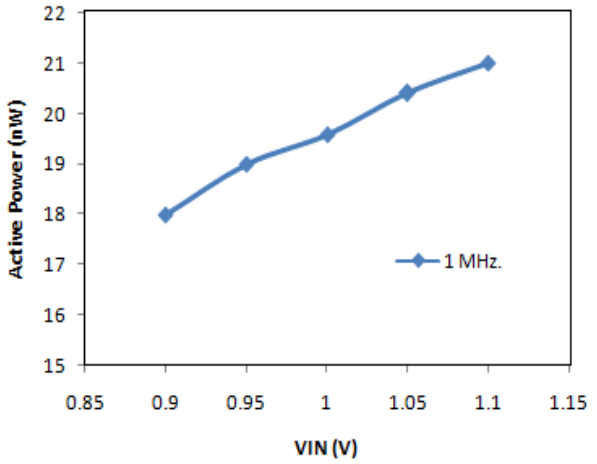

Figure 6 (b): At constant VDDL=0.4V

4.3 Comparative analysis with other designs

In this segment, the proposed TVLS is contrasted and three other references outlines. The similar investigation is indicated in Table II. The normal power consume by TVLS for up movement and down movement is just 24.7145nW, normal delay of up and down is just 2.053ns and it is contrasted and other reference papers [5], [6], [7] and [8]. The power & delay requirements are considered at a frequency of 1MHz, VDDL=0.4V and VDDH=1V. The circuit has gained the normal power utilization as low as 29.83nW in level up movement and 19.599nW in level down movement operations. Delay in the level up movement is 1.2293ns and 2.8775ns in level down movement is accounted for, these qualities are lower contrasted and other seat imprint plans. The performance qualities like power, delay, and area are superior to the past existing techniques.

The outline proposed in [6] likewise performs just up movement and static power consumed is 6.6nW with delay of 18.4ns utilizing 90nm technology. The outline proposed in [7] additionally performs just up movement and the normal power expended is 90nW with delay of 10ns utilizing 130nm innovation. The working frequency utilized as a part of outlines [5], [6], and [7] is 1MHz. The outline proposed in [8] likewise performs just up movement and the normal power devoured is 58nW with delay of 1000ns utilizing 350nm innovation with working frequency of 10 KHz.

Table 1: Performance analysis of TVLS

Type of shift	*Average Power (nW)*	*Delay (nS)*	*Energy (pJ)*
Up	29.83	1.2293	0.019
Down	19.59	2.8775	0.029

Table 1: Comparative Analysis of Level Shifters

Work/Reference	*Shift type*	*Technology*	*Power (nW)*	*Delay (ns)*
Proposed	Up & Down	90nm	Pa=24.71	2.05
[5]	Up & Down	65nm	Ps=15	15
[6]	Up	90nm	Ps=6.6	18.4
[7]	Up	130nm	Pa=90	10
[8]	Up	350nm	Pa=58	1000

Pa- Active power, Ps- Static power

5. CONCLUSION

The outline of new TVLS is with just 9 no. of transistors is utilized to perform both here and there movement operations. The circuit is developed such that it performs both level up movement and level down movement relying on the given data voltage. This novel TVLS circuit setup offers low power dispersal and low delay. The composed circuit has the capacity move 0.4V to 1V and the other way around and its reenactment results are additionally acquired. The proposed configuration is having give or take half better power productivity contrasted and the best seat imprint plan [9]. Further power and delay proficiency can be achieved with multi-Vt transistors.

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