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# Design and analysis of self clocked flip-flop based shift registers using 90 nm CMOS technology

***Achyut pandey[1], Ravi Mohan[2], Vivek Dubey[3]***
Department of Electronics and communication
Sri Ram Institute Of Technology, Jabalpur, India.

***ABSTRACT***

*This paper enumerates the efficient design and analysis of 4 bit shift registers using self clocked D flip-flop as a storage element. Self clocked flip-flop utilize internal clock generation mechanism, due to this it doesn't require external clock synchronization. It is designed by utilizing relatively less number of transistors than conventional designs, which results in drastic improvement of power performance, package density and speed. Here self triggered D flip-flop is used in order to design Serial In Serial Out(SISO), Serial In Parallel Out(SIPO), Parallel In Serial Out(PISO) and Parallel In Parallel Out(PIPO) shift registers. The shift registers presented here requires comparatively less die area, reduced power consumption and high speed than conventional shift registers. Design and simulation of shift registers have been carried out using Microwind design and simulation tool using 90nm CMOS process.*

***KEYWORDS*** *– Self clocked, CMOS, die area, power consumption, shift registers*

## I. Introduction

A register is a group of flip-flops that is required to store binary information. Each flip-flop is a binary cell which is capable of storing one bit of information. An n bit register is composed by n flip-flops and is capable of storing n bits [1]. In addition to flip-flops, register may have combinational gates that perform certain data processing tasks to control that when the new information is transferred into the register.

Registers are broadly classified into buffer or storage registers and shift registers. Storage registers have provision to store the data and making it available when required where as shift registers are capable to store the data and shifting its binary information either to right or to the left. In shift registers the flip-flops are connected in cascade configuration, with input of one flip-flop connected to the input of next flip-flop. All flip-flops are triggered by a common clock pulse which enables the shift operation in register.

This paper explains an innovative approach towards the design and implementation of shift registers using a highly efficient self triggered flip-flop. The paper is organized as follows: section II gives a brief introduction of self triggered flip-flop. In section III different configuration of shift register is discussed. Design and simulation of shift registers are presented in section IV, then paper ends in section V with major conclusion.

## II. Self triggered flip-flop

Flip-flops are the basic building block of shift registers. Here we are proposing the design of shift registers using self edge triggered flip-flops proposed in [2]. Self edge triggered flip-flop is formed by using a positive edge triggered latch along with the comparator. The CMOS implementation of self edge triggered flip-flop is shown in fig. 3, here self-triggered flip-flop depicts that unlike other flip-flops it does not require external clock pulse for synchronization. This flip-flops itself derive the clock which triggers the flip-flop internally.

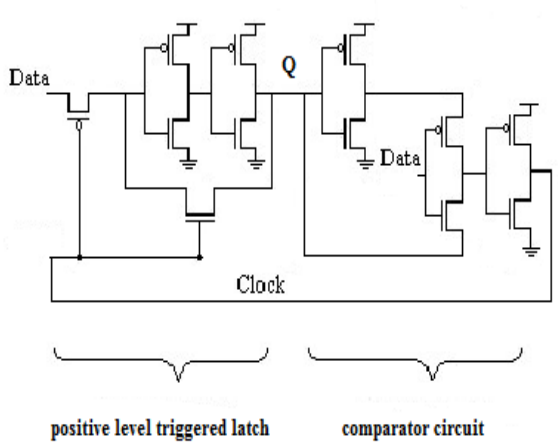



**Fig. 1:** self triggered flip-flop

The circuit is designed by a level triggered latch and a comparator. The comparator is used to provide feedback control to the flip-flop. The D latch changes its state on positive level of clock pulse only when the data input D and Latch output Q is dissimilar. When they are identical, the output remains unchanged. This fact can be utilized in order to track those instances when data D and output Q are different. A comparator is used to compare the present input and present output. Hence the comparator provides the output 1 whenever the data D and output Q attains different logic values and 0 at all other time. This output of comparator is applied as a clock signal for latch. Since the propagation delay between the input and output of latch is very small, the pulse-width of clock is

also small. Clock pulse will be available at rising as well as trailing edge of data signals. The frequency of the clock depends upon the data rate of the input D. As input data rate increases, clock frequency also increases, similarly reduction in input data rate causes reduction in clock frequency.[2]

## III. Shift Registers

Shift register is a class of registers in which data shifts or transfers from one flip-flop to another. It performs two functions data storage and data transfer. Depending upon the manner in which the input is given and output is retrieved Shift registers are classified in four categories.[3]

1) *Serial In Serial Out (SISO) Shift Register.*
2) *Serial In Parallel Out (SIPO) Shift Register.*
3) *Parallel In Serial Out (PISO) Shift Register.*
4) *Parallel In Parallel Out (PIPO) Shift Register.*

The Serial in Serial out (SISO) shift register is formed by cascading four flip-flops in such a manner that the output of one flip-flop is connected to the input of another flip-flop. It accepts the data serially and output is also retrieved serially from the output of last flip-flop. The block diagram of SISO shift register is shown in fig 2.

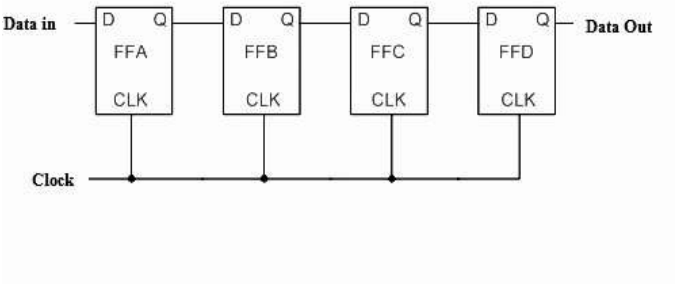



**Fig. 2:** SISO Shift Register

The serial in parallel out (SIPO) shift register accepts the data serially and the 4 bit output is obtained at the output of each flip-flop. The block diagram of serial in parallel out shift register (SIPO) is shown in fig 3

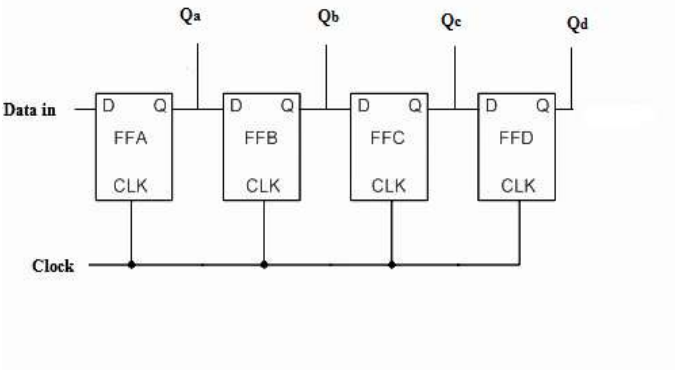



**Fig. 3:** SIPO Shift Register

The parallel in serial out shift register (PISO) loads input data bits simultaneously to the input of each flip-flops whereas output is produced at the output of last flip-flop. A multiplexer is commonly used to perform load and shift operation when required. The block diagram of parallel in serial out shift register is shown in fig. 4.

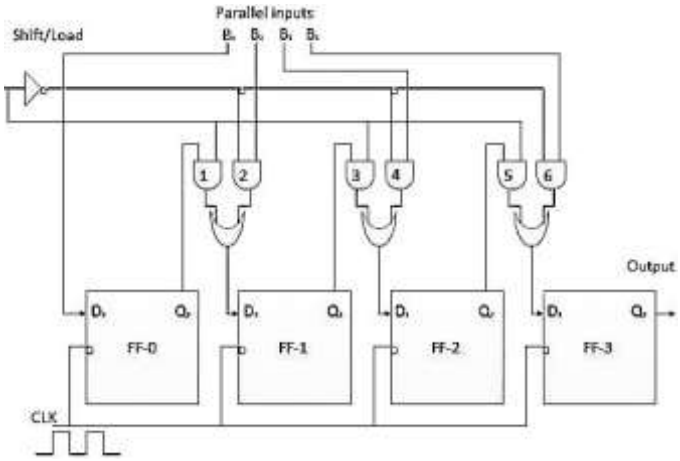



**Fig. 4:** PISO Shift Register

In parallel in parallel out shift registers input data bits are made available at the input of each flip-flop and appear at parallel output at each clock pulse. The block diagram of parallel in parallel out shift registers (PIPO) is shown in fig. 5.

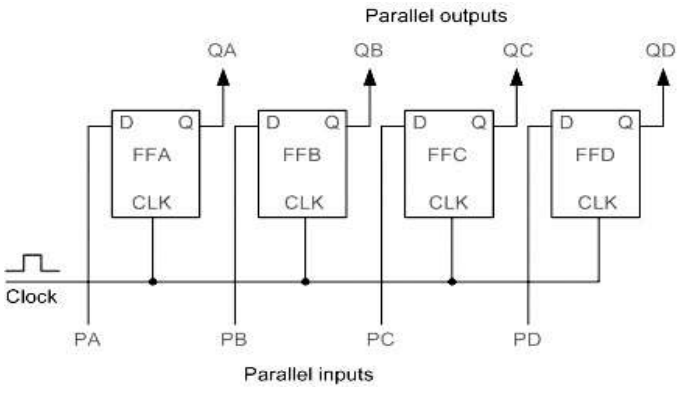



**Fig. 5:** PIPO Shift Register

Shift registers are widely applicable in various areas of digital logic. It is generally used as a converter between serial and parallel interfaces. Besides this it is also used as pulse extenders. It also involves in microprocessors and microcontrollers shift instructions. A very large numbers of serial in serial out shift registers were used as a earlier delay line memories. [4]

Shift registers are sometimes used as a time delay device and a sequencing device. The amount of delay is controlled by the number of stages in shift registers and the clock frequency. It can be implemented as Random pattern generator, ring counter and Johnson counter.

## IV. Simulation Results

this paper proposes the design and analysis of shift registers using self triggered flip-flop proposed in [2]. The layout is designed using back end design and simulation tool MICROWIND with 1.20 volt supply voltage at 27$^{o}$C temperature.

The CMOS layout of Serial In Serial Out (SISO) shift register is shown in fig. 6.

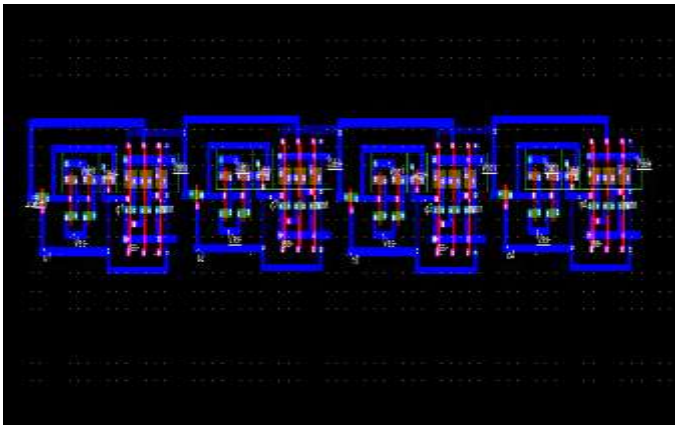


**Fig. 6:** Layout of SISO Shift Register

The simulation result of 4 bit Serial In Serial out shift registers (SISO) is shown in fig. 7. The simulation of SISO is carried out using 90nm CMOS technology with 0.1 picoseconds step size at 50 ns time scale.

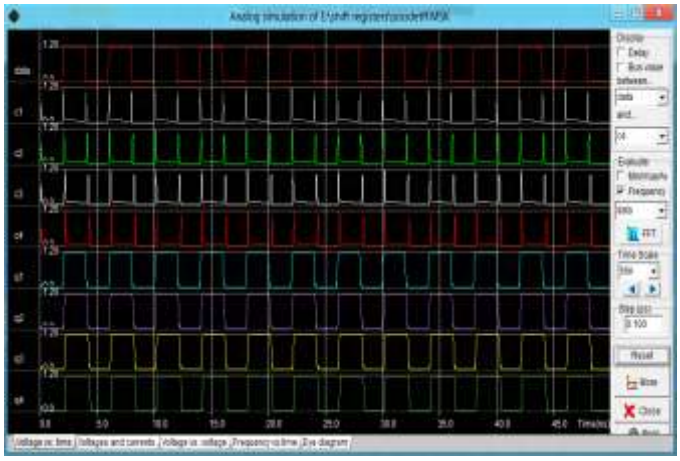


**Fig. 7:** Simulation results for SISO

The simulation is carried out at 0.25 GHz data frequency. At this data rate propagation delay between input and output is 257 picoseconds and average power consumption is 107 microwatts.

The next one is Serial in Parallel Out (SIPO) shift register. The layout of SIPO is presented in fig. 8. Layout is designed at 90nm CMOS technology using 0.1 picoseconds step size at 50 nanoseconds time scale.

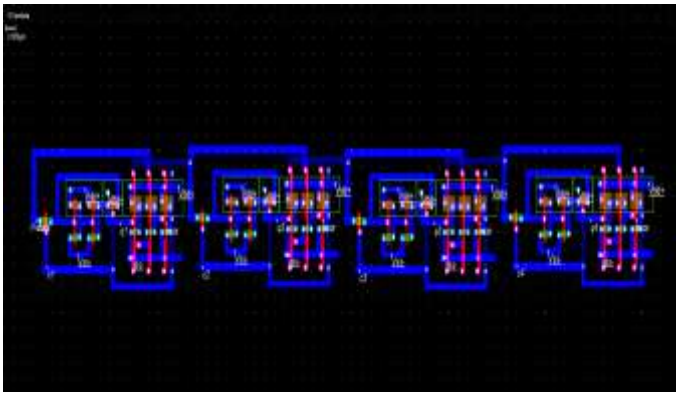


**Fig. 8:** Layout of SIPO Shift Register

The above layout is simulated using microwind simulation tool. The input data rate is 0.50 GHz and the average power consumption is 182 microwatts. The simulation result of SIPO shift register is shown in fig. 9.

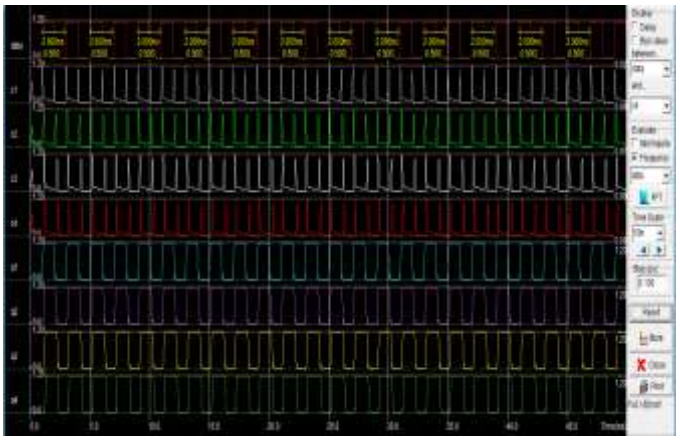


**Fig. 9:** Simulation results for SIPO

The next category of shift register is Parallel in Serial out (PISO) shift register, it takes the 4 bits data input in parallel manner and generates output in serial manner. The layout of PISO is shown in fig. 10.

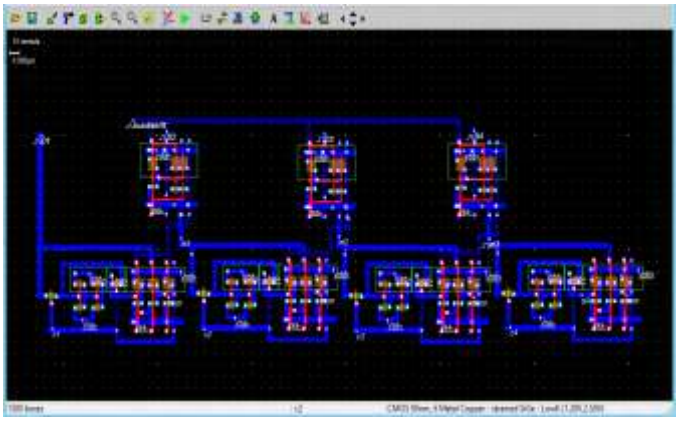


**Fig. 10:** Layout of PISO Shift Register

The simulation result of PISO shift register is shown in fig. 11. From the simulation result it is evident that the power consumption of shift register is 155 microwatts at a simulation length of 50 nanoseconds with 0.1 picoseconds step size.

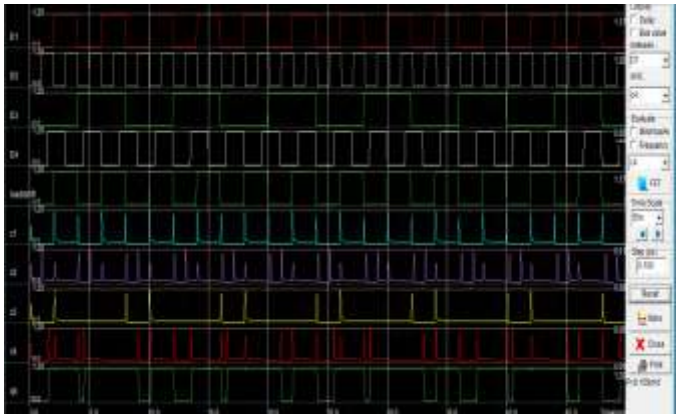


**Fig. 11:** Simulation Results of PISO Shift Register

The CMOS layout of parallel in Parallel Out (PIPO) is shown in fig. 12. It accepts the input and produces the output in parallel manner.

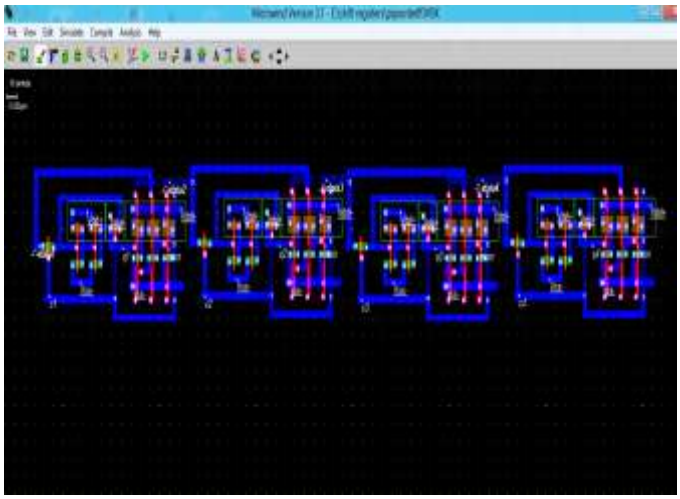
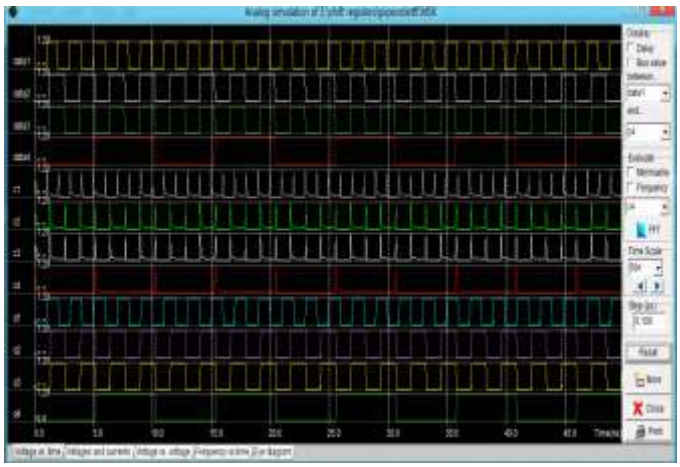


**Fig. 12:** Layout of PISO Shift Register

The PIPO shift register is simulated using microwind tool at optimum standards. The simulation result is shown in fig. 13, which illustrates the behavior of PIPO shift register.



From the above simulation result it is clear that the circuit consumes an average power of 123 microwatts at simulation length is 50 nanoseconds with 0.1 picoseconds step size.

## V. Conclusion

A high performance shift registers based on self triggered flip-flop have been proposed and simulated in microwind simulation software using 90nm CMOS technology. Self triggered flip-flop offers the best features of self edge triggered flip-flop and double edge triggered flip-flop. Above analysis shows that all types of shift registers can be designed using self triggered flip-flop. As seen in [2] it does not requires external clock pulse for synchronization, hence it consumes relatively less power than conventional designs. By this it is evident that Shift registers that are formed by self triggered flip-flop offers improved performance than conventional designs in terms of compactness speed and power consumption.

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