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# Design and Analysis of Folded Cascoded Operational Trans Conductance Amplifier

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**Abstract**
This paper presents an optimized methodology to folded cascode operational transconductance amplifier (OTA) design. In this design all the CMOS are in saturation region in order to optimize MOS transistor sizing. Using 0.18µm CMOS process, a fully differential folded cascode architecture has been proposed which attains the DC gain of 67.5Db, a unity-gain frequency of 500MHz, power dissipation is 125.56 µW, Phase Margin is 170degree, CMRR is 127.6dB and slew rate is 27.4 V/µs.

**Keywords—**Operational trans conductance amplifier (OTA); CMRR; Slew rate; power dissipation; DC Gain.

## 1.INTRODUCTION

Operational Transconductance Amplifier (OTA) is an important part of many analog and mixed signal systems. The topology of OTA's is a critical role in the design of low power system. The design of OTA continues to pose challenge as the supply voltage and transistor channel length scale down with each newer generation of CMOS technologies. The OTA is the versatile building block of any analog processing system. Designing these building blocks in terms of gain, power consumption and gain bandwidth product efficiently is still a challenging task. Operational Transconductance Amplifiers are mainly classified into Single ended output OTA's and Differential ended output or Fully Differential OTA's. In this paper, fully differential folded cascaded OTA's is discussed and their performances are compared with reference paper. Cascode current mirror load are used as a load.

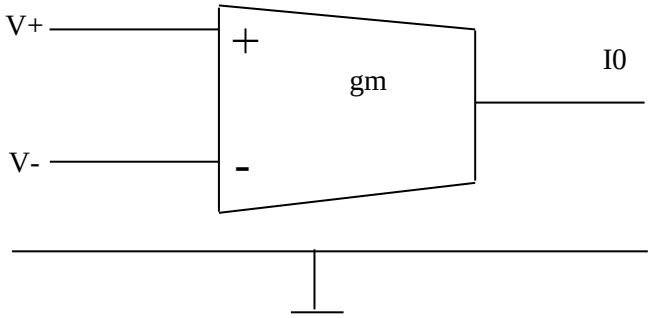


**Fig.1** Basic block diagram of OTA

The fully differential OTA's have several advantages over single-ended output OTA's such as a stable input common mode voltage, reduced harmonic distortion, doubling of the output voltage swing and suppression of coupled noise[1].

Operational Transconductance amplifier (OTA) can be considered as an exclusive case of Op-Amp in Voltage controlled current source form. An OTA which is basically a voltage to current transducer (VCT) has been receiving considerable attention due to its usefulness and versatility in many filtering and signal processing applications [2][3]. Folded cascaded is used to improve the OTA performances in terms of gain, slew rate, gain bandwidth product and power dissipation [4].

It is very crucial to design an amplifier with both high bandwidthand high gain. For high gain amplifier we use multi-stage designs, or cascade structures with long channel length transistors biased at low current levels. For high bandwidth amplifiers use single-stage designs with short channel length transistors biased at high current levels [5]. The design procedure is based on the following main parameters: DC gain,unity gain-bandwidth (UGB), input common mode range (CMR), load capacitance ($C_L$), power dissipation, Phase margin, and common mode rejection ratio (CMRR) [6].The proposed OTA in this paper describes in detail on ways to enhance DC gain for the many application [7].

This paper is organized as follows folded cascoded OTA is described in section 2, simulation result in section 3. Section 4 presents the some concluding remarks are provided.

## 2. FOLDED CASCODED OTA

The name "folded cascode" comes from folding down n-channel cascode active loads of a differential pair and changing the n-channel MOSFETS to p-channels[8].

**Table. 1** Device sizes of proposed OTA

| Parameters | Values |
|---|---|
| $C_L$ (pF) | 2 |
| Vb3(m) | -944.87 |
| $V_{dd}/V_{ss}$ (V) | ±1.8 |
| Vb4(m) | 600.42 |
| Vb2(m) | -6.947 |

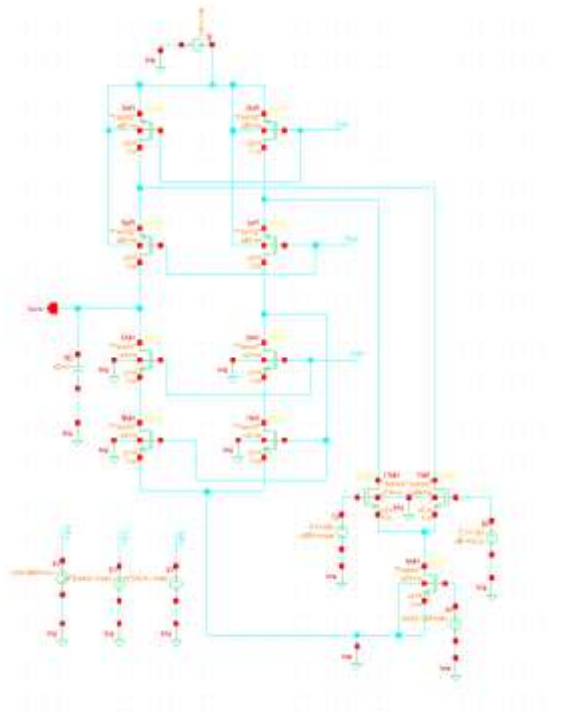

**Fig. 2** Folded cascoded OTA structure

**Table. 2** The specifications of the circuit.

| Transistors | Width(um) | Length(um) |
|---|---|---|
| PM0-PM1 | 10 | 2 |
| PM2-PM3 | 10 | 1 |
| NM2-NM3 | 4 | 1 |
| NM0-NM1 | 4 | 0.18 |
| NM7 | 4.0 | 2 |
| NM11 | 4.7 | 2 |
| NM9 | 15 | 2 |

## 3. SIMULATION RESULT

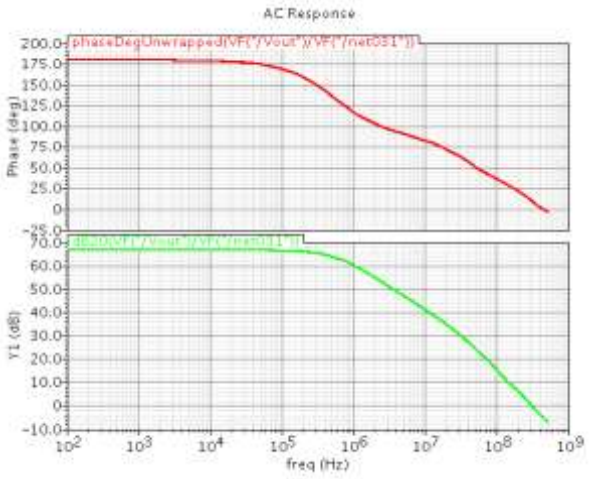


**Fig.3** Frequency response of OTA

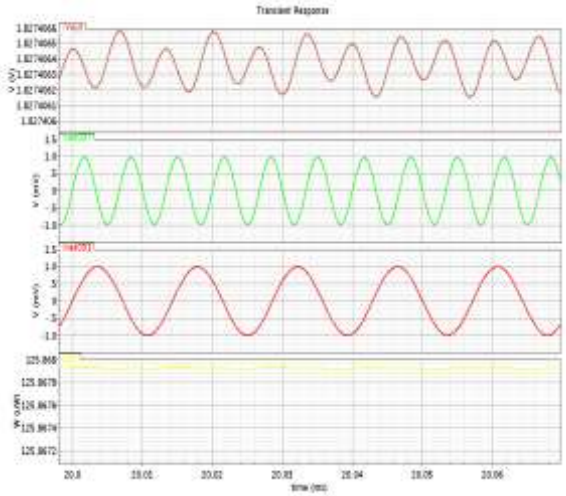

**Fig. 4** Transient response of OTA

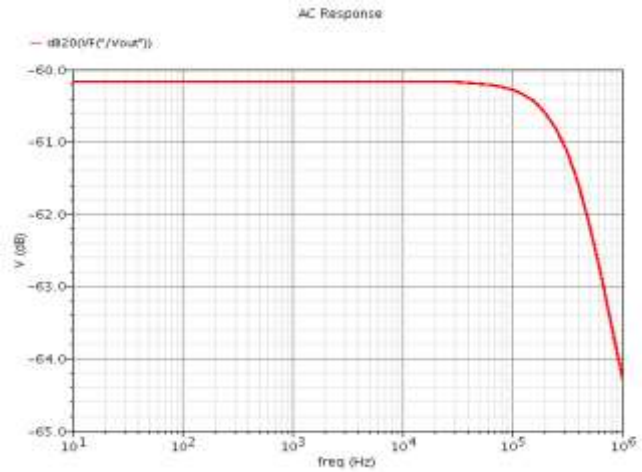


**Fig. 5** AC response with CM input range

CMRR = DC gain – CM gain

` = 67.5 -(-60.1) =127.6dB.

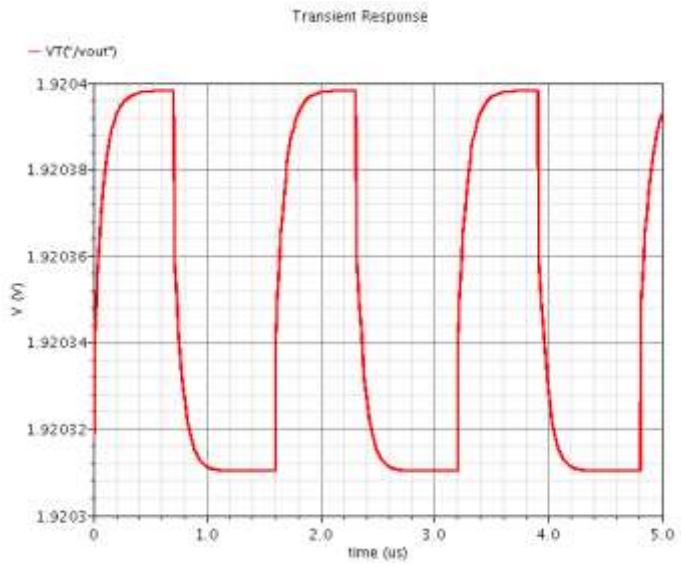


**Fig. 6** Transient response for slew rate calculation

SLEW RATE is defined as the rate of change of the voltage per unit time. It is generally expressed in units of V/µs.The slew rate is calculated by taking average of raising and falling slope [9]. The slew rate is 27.4V/µs.

| Parameters | Conventional OTA [6] | Proposed OTA |
|---|---|---|
| Gain (dB) | 61.41 | 67.5 |
| UGB (MHz) | NA | 500 |
| PM (degree) | 100.21 | 170 |
| CMRR (dB) | not given | 127.6 |
| Supply voltage | 0.7 | 1.8 |
| Power Dissipation(µW) | 235.25 | 125.56 |
| Slew Rate (V/µs) | not given | 27.4 |
| Technology | 0.045µm CMOS | 0.18 µm CMOS |

## 4. CONCLUSION

Consequently, the synthesis of high-performance analogintegrated circuits constitutes a complex activity requiring the command of many concepts. As a result, the analog designer remains a rare and highly-valued engineer worldwide. This contribution presents the strategy design of folded cascode OTA in the tsaturation region, so, the goal to reach high gain and large bandwidth has been fulfilled. Future work would involve the exploitation of these results on folded cascode OTA for all region,low consumption and wide bandapplications to use it in wide band analog-to-digital converters.

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