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A Novel High Performance Enhanced Pulse Triggered Flip Flop

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Abstract—In This paper, a novel high performance pulse Triggered flip- flop design is presented. The proposed design reduces the number of transistors stacked in the discharging path and also reduces the overall switching delay. A conditional pulse-enhancement technique is devised to speed up the discharge along the critical path only when needed. The proposed EPTL avoids unnecessary internal node transitions to improve the power consumption as compared to previously circuit. We also design 16-bit Shift Resistor using proposed EPTL. The proposed design features the best power consumption and power-delay-product performance as compared to the other three previously designed FF's. Its maximum power saving compared to the conventional P-FF designs is up to 20% and 16bit shift resistor has 39% power saving compared to previous EPTL based Shift register

Key words: IPDCO, SCCER, EPTLFF & Shift Registers

I. INTRODUCTION

Flip-Flops (FFs) or latch is the basic storage elements used extensively in all kinds of digital designs. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. One latch or Flip-Flop can be store one bit information. Some of these flip-flops are quite good at being low power and high performance Pulse triggered flip flop (PFF) is considered as a popular alternative to the conventional master slave based FF in the application of high speed operations [2]–[3]. High performance flip flops are key elements in the design of contemporary high-speed integrated circuits. In these circuits, high clock frequencies are generally gained by using a fine grain pipeline in which only few logic levels are inserted between pipeline stages.

In this paper an Enhanced Pulse Triggered Flip Flop (EPTLFF) is proposed that has reduced the number of transistors and avoids unnecessary internal node transitions, as well as reduce power consumption and delay compared to conventional P-FF (like as Ip-DCO, SCCER Previous EPTL).

II-CONVENTIONAL P-FF DESIGNS

Some conventional P-FF designs, which are used as the reference designs in later performance comparisons, are reviewed.

1.1- IP-DCO: Implicit Pulsed Data Close To Output [6]

Fig.1 shows the IP-DCO, it consists of pulse generator and semi dynamic latch structure [6]. An IP-DCO is one of the implicit kinds of flip-flop where the pulse is generated inside the flip-flop itself. Here the input node is kept closer to the output node so that it has less data to output delay, hence the name DCO. Here the clock signal and complement of the clock signal generates a narrow pulse of short duration.

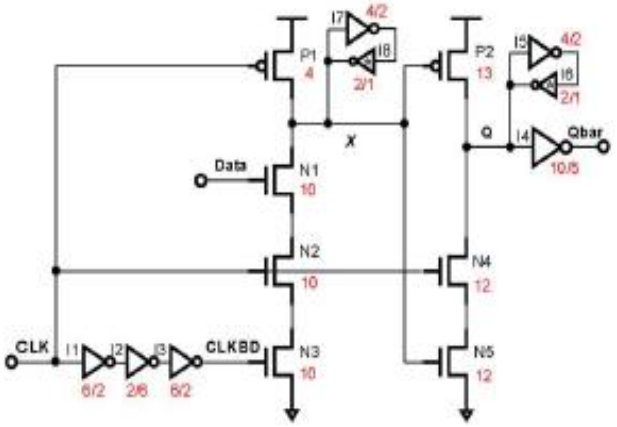

Fig 1. Conventional pulse-triggered FF designs. (a) IP -DCO [6]

1.2-SCCER: Single- Ended Conditional Capture Energy Recovery [9]

Fig. 2 shows a refined low power P-FF design SCCER using a conditional discharged technique .In this design, the keeper logic (back-to-back inverters I7 and I8 in Fig. 1) is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node X [9]. The discharge path contains NMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node X, an extra NMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1" and node X is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node X can be properly discharged.

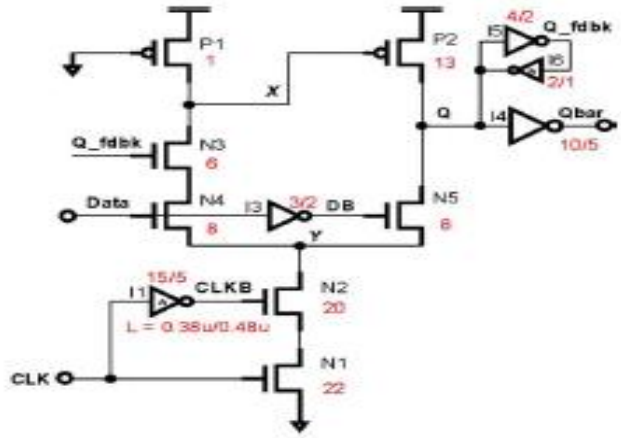

Fig 2.Conventional pulse-triggered FF designs.SCCER [9]

1.3-EPTLFF-: Enhanced Pulse Triggered Flip Flop [10]

Fig. 3 shows design Enhanced Pulse Triggered Low-power Flip Flop (EPTLFF), for high-speed operation of data storage and a popular alternative to Master slave flip-flop. The enhanced pulse triggered low-power flip flop (EPTLFF) with pulse control scheme consists of pulse generator for generating Strobe signals and a latch for data storage. The upper part latch design and lower part enhanced pulse generation. This particular clock pulse is used to a two-input pass transistor logic, N2, N3 a two-input pass transistor logic based AND gate to control the discharge of transistor N1. Author design reduced the discharging path X, avoids unnecessary internal node transitions to reduce power consumption and delay.

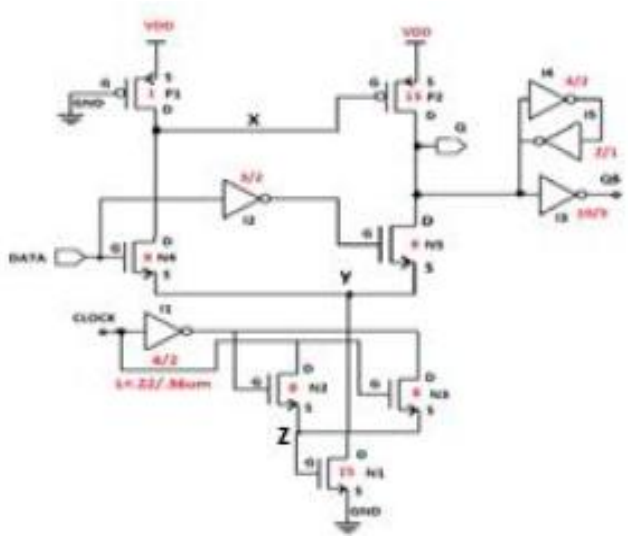

Fig 3.Conventional pulse-triggered FF designs. EPTL [10]

III- PROPOSED Enhanced Pulse Triggered Flip Flop (EPTLFF)

Fig. 4 shows our proposed design Enhanced Pulse Triggered Flip Flop (EPTFF), for high speed operation of data storage and a popular alternative to Master slave flip-flop. The enhanced pulse triggered low-power flip flop (EPTLFF) with pulse control scheme consists of pulse generator for generating Strobe signals and a latch for data storage. It reduces the number of transistors stacked in the discharging path and also reduces the overall switching delay.

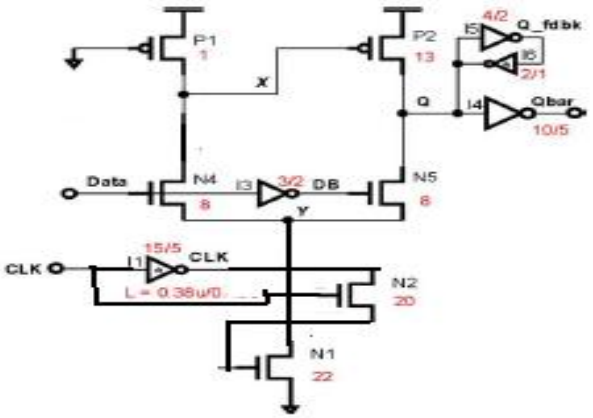

Fig. 4 Proposed Enhanced Pulse Triggered Flip Flop

Refer to Fig. 3, the upper part latch design and lower part enhanced pulse generation. This particular clock pulse is used to input pass transistor logic, N2 input pass transistor logic to control the discharge of transistor N1. The output node Z is kept at zero most of the time. At the rising edges of the clock, transistors N2 is turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1.The switching power at node Z can be reduced due to a diminished voltage swing. Where the discharge control signal is driven by a single transistor, conduction of one NMOS transistors (N2) speeds up the operations of pulse generation. In this design reduced the discharging path X, avoids unnecessary internal node transitions to reduce power consumption and power delay product.

IV- Shift Registers

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states. All flip-flops are driven by a common clock. There are different kinds of shift registers.

Parallel in Parallel out Shift Register

For parallel in parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a 16-bit parallel in parallel out shift register constructed by proposed EPTL D flip-flops and shown in fig. 5.

V- Comparison Result

The comparison of result summarizes some important performance indexes of these P-FF and 16 bit shift resistor designs as shown in Table 1, 2, 3, 4. These include transistor count, Area, D to Q & D to Qbar Rising, Falling, propagation Delay, Power consumption and power delay product in 180-nm technology.

Table 1. 1-BIT D flip flop for Q output

Flip Flop	Transistor	Rising Delay (*)	Falling Delay(*)	Propagation Delay-(*)	Power Consumption ($)	PDP (&)
EPTL(Prop)	16T	18	24	21	.556	11.67
EPTL	17T	17	23	20	.692	13.84
SCCER	17T	29	8.9	.005	1.1	.0055
IDPCO	23T	26	24	25	2.3	57.5
Unit: *= ns, $= ps & = nsxps						

Table2. 1-BIT D flip flop for Q output

D Flip Flop	Transistor	Rising Delay (*)	Falling Delay(*)	Propagation Delay-(*)	Power Consumption($)	PDP (&)
EPTL(Prop)	16T	18	24	21	.556	11.67
EPTL	17T	18	24	21	.692	14.53
SCCER	17T	.007	24	.047	1.1	.051
IDPCO	23T	18	24	21	2.3	48.3
Unit: *= ns, $= ps & = nsxps						

Table 3. 16 BIT PIPO shift resistor for Q output

PIPO using Flip Flop	Transistor	Rising Delay (*)	Falling Delay(*)	Propagation Delay-(*)	Power Consumption ($)	PDP (&)
EPTL(Prop)	256T	51	51	51	19	969
EPTL	17T	50	50	50	31	1550
SCCER	17T	50	50	50	23	1150
IDPCO	23T	17	17	17	52	864
Unit: *= ns, $= ps & = nsxps						

Table 4.16 BIT PIPO shift resistor for Qbar output

PIPO using Flip Flop	Transistor	Rising Delay (*)	Falling Delay(*)	Propagation Delay-(*)	Power Consumption ($)	PDP (&)
EPTL(Prop)	256T	45	54	49.5	19	940.5
EPTL	289T	45	54	49.5	31	1534.5
SCCER	289T	54	45	49.5	23	1138.5
IDPCO	529T	12	21	16.5	52	858
Unit: *= ns, $= ps & = nsxps						

IV-Simulation Result

To evaluate the performance, shift registers discussed in this paper are designed using 180-nm CMOS technology. All simulations are carried out using Tanner Tools. Flip-flop based parallel in Parallel out Shift Register Schematic design in Software Tanner Tools is shown in fig. 5(a). (b) & (c).

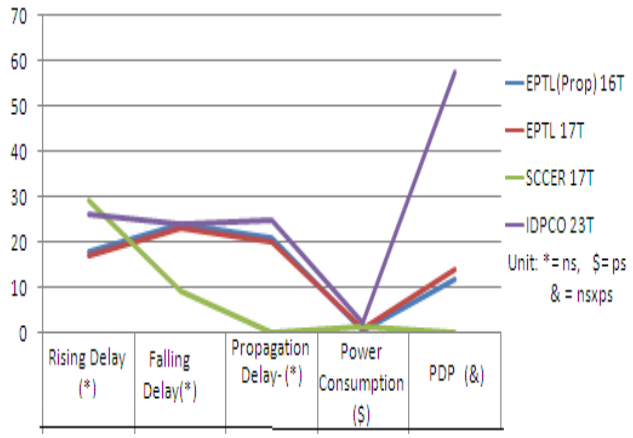

Fig.5 (a) 1-BIT flip flop for Q output

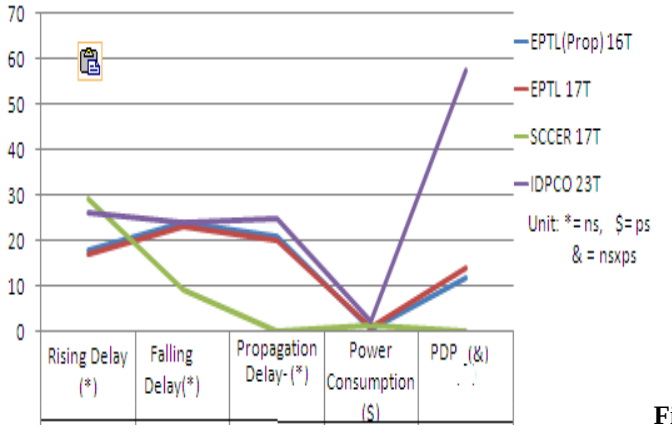

Fig . .5 (b) 1-BIT flip flop for Qbar output

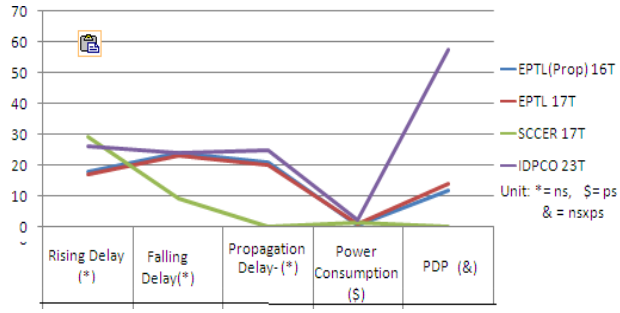

Fig. .5 (c) 16-BIT Shift Resistor for Q output

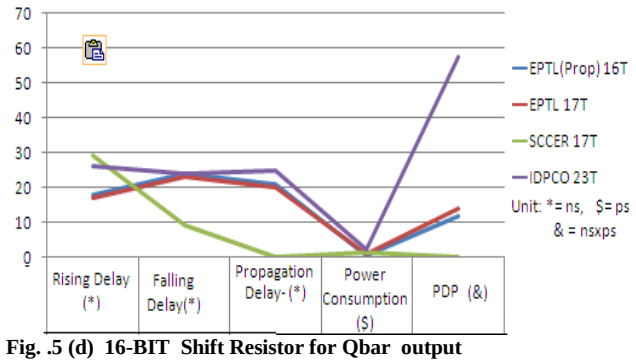

Fig. .5 (d) 16-BIT Shift Resistor for Qbar output

Conclusion

In this paper, the various Flip Flop designs like, IP- DCO, SCCER, EPTLFF and proposed EPTLFF are discussed. The enhanced pulse triggered Pass transistor logic Flip Flop (EPTLFF) design successfully reduces the number of transistors stacked along the discharging path by incorporating simple pass transistor logic. The EPTLFF avoids unnecessary internal node transitions to reduce power consumption and also design a16 bit shift resistor based on proposed EPTLFF. Simulation results indicate that the proposed design excels rival designs in performance indexes such as power, D to Q delay. With all these results proposed EPTLFF speed performance and power are better than Ip DCO, SCCER and previous EPTLFF designs.

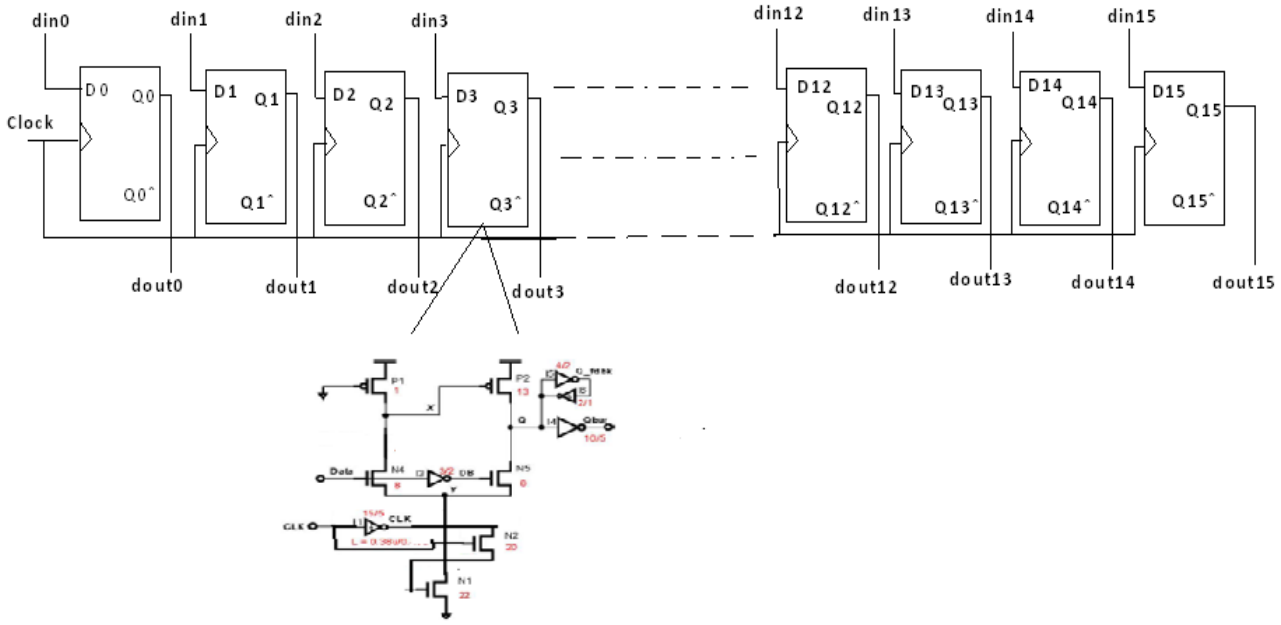

Fig.5 16 Bit Shift resistor using proposed EPTL

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