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Design and Analysis of Combinational Circuits Using Quantum Dot Cellular Automata (QCA)

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ABSTRACT: Quantum Dot Cellular Automata (QCA) is one of the emerging trends in the field of nanotechnology which help to overcome the limitations of CMOS technology. QCA is simple in structure having significantly lesser elements as compared to CMOS design. It has the potential for attractive features such as faster speed, smaller size and low power consumption than transistor based technology. Quantum-dot cellular automata have a simple cell as the basic element. The cell is used as a building block to construct gates, wires, and memories. By taking the advantages of QCA are able to design interesting computational architectures. Unlike conventional computers in which information is transferred from one place to another by means of electrical current, QCA transfers information by propagating a polarization state. This paper proposes a detailed design and analysis of combinational circuits such as half adder, full adder and decoder for quantum-dot cellular automata.

KEYWORDS: QCA, half and full adder, decoder, majority gate.

I. INTRODUCTION

A.QCA cell

A quantum-dot cellular automata (QCA) is a square nanostructure of electron wells confining free electrons. Each cell has four quantum dots which can hold a single electron per dot. The four dots are located at the corners of the cell and only two electrons are injected into a cell. By the clocking mechanism, the electrons can tunnel through to neigh boring cells during the clock transition by the interaction between electrons. A high potential barrier at the settled clock signal locks the state and results in a local polarization which is determined by Coulombic repulsion. The two electrons reside in opposite corners so that two polarizations are possible as seen in Fig. 1. Those two binary states can be used to make QCA cell[1] a storage cell, a computing cell, or a wire.

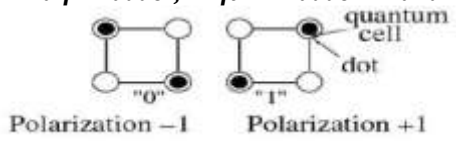

Figure.1 QCA Cell

B. Signal flow

A series of QCA cells act like a wire. An illustration of a QCA wire is shown in Fig. 2. During each clock cycle half of the wire is active for signal propagation, while the other half is stable. During the next clock cycle, half of the previous active clock zone is deactivated and the remaining active zone cells trigger the newly activated cells to be polarized. Thus signals propagate from one clock zone to next.

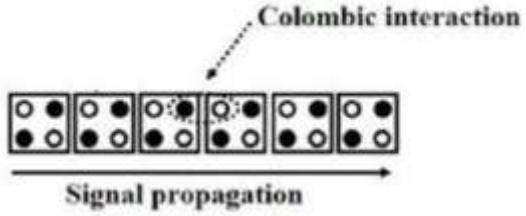

Figure.2

Signal Flow

C.QCA Clock

The circuit area is divided into four sections and they are driven by four phase clock signals. As shown in Fig. 3, there is a 90 degree phase shift from one section to the next. In each clock zone, the clock signal has four states: high-to low, low, low-to-high, and high. The cell begins computing during the high-to-low state and holds the value during the low state. The cell is released when the clock is in the low-to-high state and inactive during the high state.

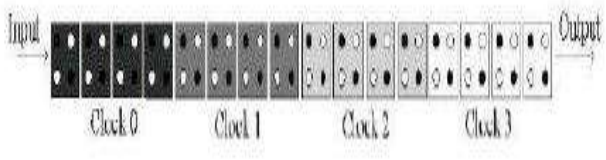

Figure.3 Clock Zones

The QCA clocking [3] signal is used to control the signal propagation along the QCA cells arrangement. There are Four-Different Clocking Phases such as „SWITCH, HOLD, RELEASE and RELAX".

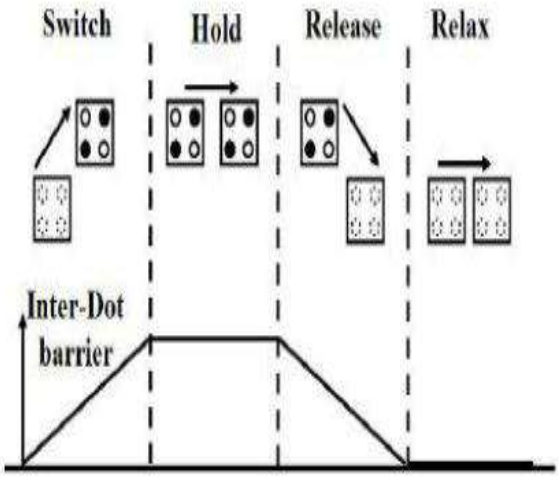

Figure.4 Clock Phase

SWITCH: During this phase, the inter-dot barriers are slowly raised and the computation takes place according to QCA cell arrangement.

HOLD: In this phase, the inter-dot barriers are kept high and the QCA cells retain their states.

RELEASE: During this phase, the barriers are lowered and the cells are allowed to relax to unpolarized states.

RELAX: The barriers are kept low and the cells remain in unpolarized state.

II. LOGIC GATES

Logic gates [2] are required to build arithmetic circuits. In QCA, inverters and three-input majority gates serve as the fundamental gates.

A.Majority Gate

The governing equation for the majority gate is M (a; b; c) = ab+ bc + ca. Fig. 5 shows the gate symbols and their layouts. Two input AND and OR gates can be implemented with 3 input majority gates by setting one input to a constant. With ANDs, ORs, and inverters, any logic function can be realized.

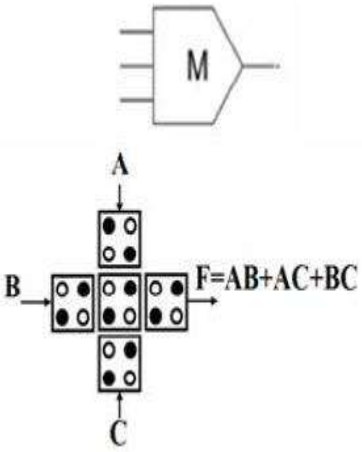

Figure.5 Majority Gate

B .QCA Inverter

QCA Inverter can be implemented in position QCA cells to invert the output from input logic level.

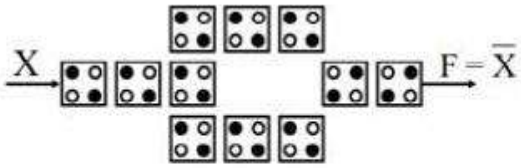

Figure.6 Inverter

III. CROSSOVER AND MULTILAYER DESIGN

In QCA, there are two crossover options. They are coplanar crossings and multilayer crossovers. It has been believed that single layer designs are possible with QCA because of the ability to create co-planner crossovers. Coplanar crossings require using two cell types (regular and rotated). The regular cell and the rotated cell do not interact with each other when they properly aligned, so rotated cells can be used for coplanar wire crossing. They have very little mutual interaction. In the coplanar crossing, rotated cells are used when two wires cross. In a coplanar crossing, there is a possibility of a loose binding of the signal which causes a discontinuity of the signal propagation and there is the possibility of back-propagation from the far side constant input. So putting enough clock zones between the regular cells across the rotated cells is required. So the complex circuits using coplanar crossover are very likely fail. As well, the crossover is extremely sensitive to fabrication errors and depends on the ability to fabricate two types of QCA cells. Therefore is presented a solution to this Problem.

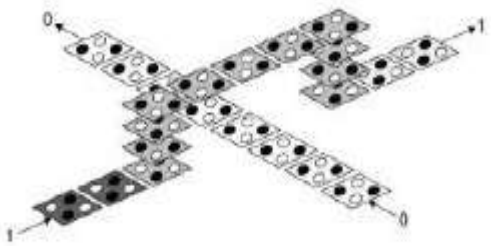

Figure.7 Multilayer design

IV. CIRCUIT IMPLEMENTATION

The QCA half adder design is shown in Fig. 8.The QCA full adder design is shown in Fig. 10.The QCA Decoder design is shown in Fig. 12 proposed QCA multiplexor has been designed and simulated using the QCA Designer [5] tool. This tool allows users to do a custom layout and then verify QCA circuit functionality by simulations. It includes two different simulations engines such as a bistable approximation and a coherence vector. The current QCA technology does not specifically set the possible operating frequency and actual propagation delays. Thus, the maximum cell count can be set as a design parameter [6].

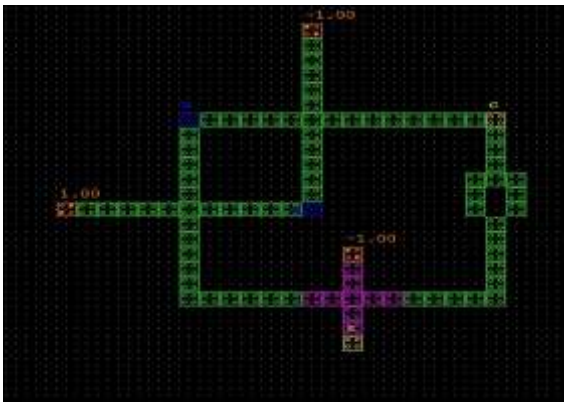

Figure.8 Half adder

A Half adder consists of two binary inputs and two binary outputs. The input variables designate the augend and addend bits; the output variables produce the sum and carry. The QCA design of half adder is used to three majority gates and one inverter shown in fig.8 and simulation result is shown in fig.9.

S = A‟B + AB„
C = AB

Expression for half adder

Sum = A_bar &B + B_bar & A = (A & B) _bar & (A + B)
Let us have X = (A & B) _bar= majority (A, B, "0'')
And Y = (A + B) = majority (A, B, "1'')
Therefore X * Y =majority (X, Y, "0'') =
Sum = majority ([majority (A, B, "0'')], [majority (A, B, "1'')], "0'')
Carry = X = (A & B) = majority (A, B, ''0'')

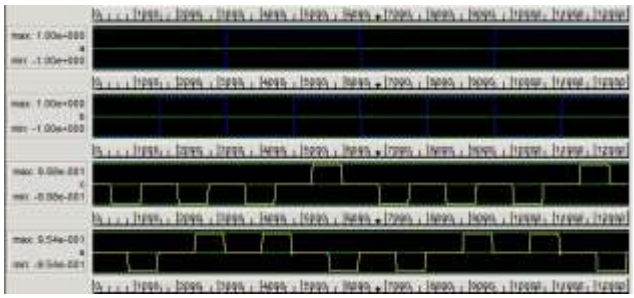

Figure.9 Simulation Output

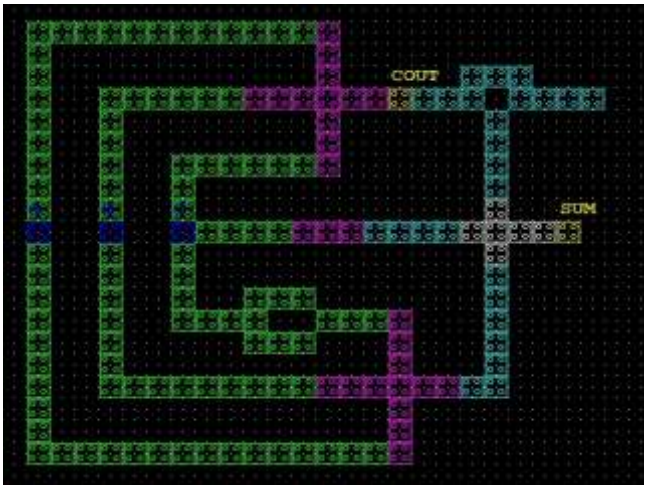

Fig.10 Full adder

A full adder is a combinational circuit that forms the arithmetic sum of three input bits. Two of the input variables, denoted by a and b, represent the two significant bits to be added. The third input c,represents the carry from the previous lower significant position. The QCA design of full adder is used to three majority gates and two inverters shown in fig.10 and the simulation result is shown in fig.11.

Expression of full adder

Sum = a'b'c + a'bc'+ ab'c'+ abc = majority[majority(a,b,c)', majority(a,b,c'),c]

Carry = ab+bc+ca = majority(a,b,c)

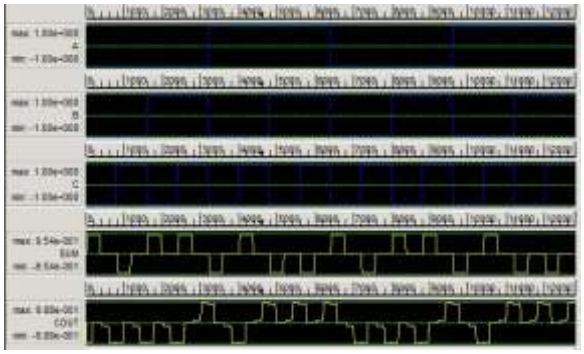

Figure.11 Simulation Output

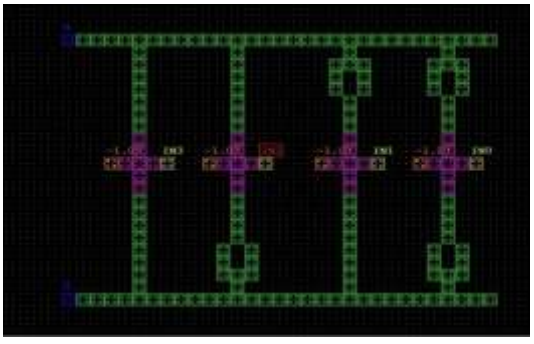

Figure.12 Decoder

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. The QCA design of decoder circuit is

used to four majority gates and four inverters shown in fig.12 and simulation result is shown in fig.13.

Expression of Decoder

B0 = majority (x', y', 0)

B1 = majority (x', y, 0)

B2 = majority (x, y', 0)

B3 = majority (x, y, 0)

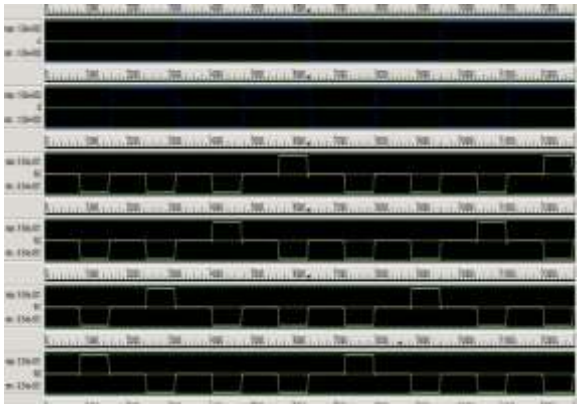

Figure.13 Simulation Output

V. SIMULATION

With QCA Designer ver.2.0.3, the circuit functionality is verified. The input and output waveforms are shown in Fig. 9, Fig.11, Fig.13 According to QCA Designer, this design has 124 cells (including input and output cells) and an area of approximately 0.25μm2 (each cell is18*nm*×18*nm* , with a 2*nm* gap between cells).

VI. CONCLUSION

This paper presents design for QCA Half adder, Full adder, Decoder. The layout is done using QCA Designer and this design is analysed according to the complexity and area. Simulation shows that occupied area for this design is 0.25m2. For future work, the design can be optimized in terms of complexity and the number of clock zones. Also, computation time and power consumption can be computed for designing.

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