SIMULINK BASED THREE-PHASE CLOSED LOOP POWER FLOW CONTROL USING TCSC

[1]D. Chatterjee, [2] A. Mitra

Department of Electrical Engineering, Narula Institute of Technology
Email: [1]deb.chatterjee88@gmail.com, [2]arkendu83@gmail.com

Abstract: As per the requirement of our power sector which is also developing with the development of other sectors, facing great challenges to meet the demand and without installing a new generating station or any tie line in extra it is also economical and suitable for the system. So if the existing system is used efficiently then the demand can be matched suitably. For this many devices, AC-DC converter etc. are used in between which FACTS devices take a large benefits to meet the system demand. In this paper, the close loop control of TCSC (Thyristor Controlled Series Capacitor) will be discussed which is simple and also suitably controlled with a different control strategy by which approximately 90-95% compensation can be done. The whole control strategy with the change of load which is done here automatically is discussed here. The total analysis is done in MATLAB Simulink.

Keywords: Closed Loop Control, Line Efficiency, Line Loss, Voltage regulation, Zero Crossing Detector.

1. INTRODUCTION

India, formally the Republic of India, is a rising country in South Asia. It is the seventh-largest country by area, the second-most overcrowded country with over 1.2 billion people, more than a sixth of the world's population. Even now comprising 17.5% of the world's population, India is predictable to be the world's most overcrowded country by 2025, surpassing China, its inhabitants reaching 1.6 billion by 2050. Its population progress rate is 1.41%, position 102nd in the world in 2010. Indian populace touched the billion results in 2000. So, the electricity demand with the demand of additional necessities is fetching supplementary significant to overgrown in the world records as a industrialized nation. The electricity demand prognostication is a vital input for planning of the power segment to come across the forthcoming power necessity of different sectors of electricity intake. A calculated load progress in industry, agriculture, domestic and other segments is essential to ensure cohesive progress in all segments of economy and therefore it is compulsory that infrastructure is scheduled in several areas of energy consumption so as to uninterrupted the inclusive growth of economy in coherent manner.

In an effort to bump into the power demands of an evolving nation-state, the Indian energy sector has countersigned a swift progress. But resource intensification and progress in energy supply have miscarried to run into the constantly growing demands due to the growing inhabitants, speedy physical growth of inner-city areas, and developing economy [1]. So Power System Engineers are towards a boundless challenge to growth the power transfer capability of the prevailing system. But rather than adding of new tie line or increasing the generation, if the transfer capability can be increased, then it can be more well-suited and operational. And it must include an extra supplementary cost which is not desirable for us. To growth the power transfer capability we have to use many devices such as many types of filters, AC-DC converter etc. Among them FACT devices are the new era to match the increasing demand used in series or shunt. By the use of series fact device the following benefits can be taken [2]

- Increase power transfer capability.
- Improve system stability.
- Reduce total system losses.
- Improve voltage profile of the lines and in total system.
- Optimize power flow between parallel lines.

Above and beyond this nature, the FACTS devices can execute various kind of operation such as transient stability improvement, power oscillation damping, sub synchronous resonances (SSR) mitigation and fault current limitation etc. [3]. So the Power Engineers are fascinated by this technique to execute a several action by make known to a device which is much cost in effect also.

The most advanced FACT device termed as Thyristor Controlled Series Capacitor (TCSC), a series compensator, consists of a series capacitor bank shunted with an inductor bank which in series with two back to back thyristor to provide a smoothly variable series capacitive reactance [4]. It can be concluded that it is the combination of a capacitor and a TCR (a reactor, series with a back to back thyristor). It can control overloading and under loading condition automatically. When the line is lightly loaded then the device will introduce inductive reactance in series with the line and under heavy loaded condition, the device will offer capacitive reactance in series with the line to enhance power transfer capability. To do this automatically with the change of load, a back to back thyristor have to be added with the reactor (TCR) which controls the overall reactance of the device. The TCSC is applied in the transmission lines for the improvement of the transmission capacity and stability. Considering the rapid development of UHV grid and the characteristic of TCSC, it can be predicted that the TCSC will be installed on the UHV transmission line in the near future [5].

The purpose of this research is to present a general overview of the closed loop control method of TCSC. The steady-state characteristics are well known from the literature and a number of dynamical models also have been presented in different papers. However, in the author's opinion, the dynamical models presented so far turn into mathematics very fast. The engineer is left without any good description making it easy to understand the dynamics of the TCSC.

2. OPERATION OF TCSC

The inductive part of the TCSC consists of a fixed inductor (preferably air-cored) of inductance L and two anti-parallel thyristors connected in series with the inductor. The thyristors are operated by simultaneous application of gate pulse to the thyristors of the same polarity. After applying the gate pulse to the thyristor, it maintains its conduction mode until the current passes through the thyristor becomes zero. In case of ac circuit, thyristor will automatically block immediately as the ac current reaches zero, till gate pulse will be applied to the thyristor further.

The main objective is to control the current through the inductor by adjusting the firing angle of the gate pulse applied to the thyristor, this will change the nature of the waveform as well as the average value of the current through series capacitor and a result voltage across the device will change. Hence, the adjustment of firing angle α plays an important role to control the TCSC voltage and current, or in other word, the effective impedance of the TCSC. So the main objective is to control the power flow automatically to get a desired value with the change of load and increase the system stability and reliability also.

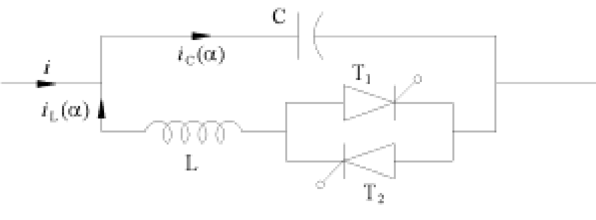


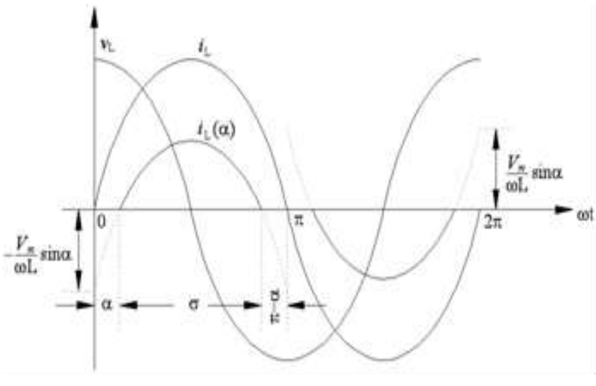
Fig.1. Basic Circuit of TCSC

Current through the reactor can be controlled from maximum (when thyristors are in full conduction mode) to zero (when thyristors are in blocking mode) by changing the delay of the firing pulse α. Since inductor current lags the voltage by 90°, the firing pulse for full conduction of the thyristors is to be applied at the peak of the voltage. Fig. 2 represents the method of controlling the inductor current both for positive and negative current half-cycles, at zero firing angle and at any arbitrary firing angle α. When gate pulse delay is α, the current in the inductor can be expressed with an applied voltage of $V_m \cos\omega t$ gives,

$$i_L = \frac{1}{L}\int_{\alpha}^{\omega t} V_m \cos\omega t dt = \frac{V_m}{\omega L}\left|\sin\omega t\right|_{\alpha}^{\omega t}$$

$$i_L = \frac{V_m}{\omega L}\left(\sin\omega t - \sin\alpha\right) \qquad (1)$$

Since the thyristors will stop conduction as current reaches zero, equation (1) is useful for conduction of hyristors within the interval of $\alpha \le \omega t \le \pi - \alpha$. The term $\frac{V_m}{\omega L}\sin\alpha$ in the equation (1) is simply an constant offset depending upon the value of α, which decreases the instantaneous value of inductor current in each positive half cycle and increases the same in each negative half cycle as shown in Fig. 2. Clearly from the Fig. 2, inductor current reaches its zero value before $\omega t = \pi$ when there is some delay (α) applied to the firing pulses and the thyristors will stop conduction. With a delay of $\alpha = 0$, the term $\frac{V_m}{\omega L}\sin\alpha$ in equation (1) vanishes and the thyristors are in full conduction mode of



operation.

Fig.2. Thyristor Controlled Inductor Current

Applying Fourier Series expansion, the average value of the fundamental current can be expressed as follows

$$I_{Lf}(\alpha) = \frac{2}{\pi}\int_{\alpha}^{\pi-\alpha}\frac{V_m}{\omega L}\left(\sin\omega t - \sin\alpha\right)\sin\omega t d(\omega t)$$

or, $$I_{Lf}(\alpha) = \frac{V_m}{\omega L}\left[1 - \frac{2\alpha}{\pi} - \frac{1}{\pi}\sin 2\alpha\right]$$

$$\therefore \qquad x_L(\alpha) = x_L\left(\frac{\pi}{\pi - 2\alpha - \sin 2\alpha}\right) \qquad (2)$$

where, $x_L = \omega L$

Now it is clear from the above equation that $x_L(\alpha)$ is a function of α and it varies as α varies. When both the thyristors are in fully conduction mode, whole sinusoidal current will pass through the inductive reactance and correspondingly the term in the expression of current $\sin\alpha$ becomes zero accordingly. Clearly this situation indicates that the firing angle of the thyristors is maintained at $\alpha = 0°$ and $x_L(\alpha)$ becomes minimum and its corresponding value will be x_L. To find the maximum value of $x_L(\alpha)$, differentiating $x_L(\alpha)$ with respect to α and make the value equals to zero, we have,

$$\frac{d}{d\alpha}\left[x_L(\alpha)\right] = 0$$

or, $$\frac{d}{d\alpha}\left[x_L\left(\frac{\pi}{\pi - 2\alpha - \sin 2\alpha}\right)\right] = 0 \qquad (3)$$

which provides $\alpha = \frac{\pi}{2}$. Putting this value in the expression of $x_L(\alpha)$, theoretically we get an infinite value of inductive reactance. So, this situation indicates that for a value of α equals to $\frac{\pi}{2}$, the inductance will offer an infinite reactance. For this value of α, no current will pass through the inductance, also the term in expression of current $\sin\alpha$ becomes 1, that indicates the peak value of the current will be subtracted from the expression of current varying sinusoidal, resulting zero current through the thyristors as well as inductor. Thus, from the above observation, $x_L(\alpha)$ can be varied within the range $x_L \le x_L(\alpha) \le \infty$ as the firing angle varies $0 \le \alpha \le \frac{\pi}{2}$.

The device TCSC shown in Fig. 1 consists of parallel combination of a capacitor and an inductor associated with two anti-parallel thyristors connected in series with the inductor. Since the effective reactance is a function of the firing angle α, the net impedance of the device will be

$$x_{TCSC}(\alpha) = \frac{x_L(\alpha)x_C}{x_L(\alpha) - x_C} \qquad (4)$$

Clearly, from the equation (4) that both the capacitive reactance and variable inductive reactance of the TCSC will offer a tunable LC circuit, where the value of $x_L(\alpha)$ can be varied from its minimum value x_L, when $\alpha = 0$ to its maximum value ∞ (infinity), when $\alpha = \frac{\pi}{2}$. At the time of maximum reactance, no current will flow through the inductive path and the entire line current will flow through the capacitor. Now decreasing the value of α, the value of $x_L(\alpha)$ goes decreasing, resulting an inductive path to bypass some of the line current through the inductor and hence the current flowing through the capacitor goes decreasing accordingly, resulting an increased value of the capacitive reactance.

At a certain instant, when $x_L(\alpha)$ will be equal to x_C, parallel resonance will occur and TCSC will offer theoretically an infinite reactance. Up to this point of compensation, TCSC will offer capacitive reactance because till the value of $x_L(\alpha)$ is higher than x_C. Compensation beyond parallel resonance, TCSC will offer inductive reactance because at this point, value of x_C will be higher than $x_L(\alpha)$. Since, current flows through the least reactive path, inductive current will be established beyond the occurrence of parallel resonance.

3. TCSC CHARACTERISTICS

From the previous discussion, the effective reactance of TCSC $x_{TCSC}(\alpha)$ operates in three region, inductive region, capacitive region and resonance region as shown in Fig. 3. Inductive region starts increasing from value $x_L \| x_C$ to infinity in resonance region and decreasing from infinity to x_C in capacitive region [18].

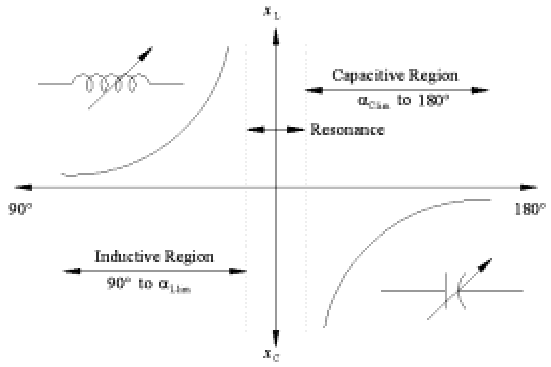


Fig.3. TCSC Operating Regions

4.

4. DESIGN OF CONTROLLER

In this chapter the closed loop control of TCSC with changing the load is discussed. As discussed earlier, the series FACTS devices can be used for several purposes such as power flow control, increase of transmission capability, voltage control, stability improvement, power quality improvement, power conditioning, flicker mitigation, interconnection of renewable and distributed generation and storages etc. In this project the power flow control strategy of TCSC and the voltage stability of the receiving end with enhancement of loads has been carried out.

When a load changes in a system abruptly the system power flow, voltage profile and also stability of the system gets affected which is undesirable for the system obviously. As a Power System Engineer this fluctuations are not suitable to us. With the change of load if the voltage profile abruptly change then the system will be affected in such a way that a higher protection scheme should be involved to the system. Also the power transfer will be in such a way that the system attached to that value where the system goes to the side of instability. And the main scheme is that the stability limit which should not be exceed by the system. So, to get the desired value by the system, TCSC will be introduced in such a way that we can a get a suitable value. It is a Power Electronics based Control System oriented Power System device which is added with the EHV or UHV transmission line which gives a quick response in nature with a little change of the system parameter and also system load. Here the device TCSC is connected in series with the transmission line which consists an inductor with two back-to-back thyristor is in parallel with a capacitor. If the whole systems power and as well as the voltage should be kept at a desirable value a suitable and different control strategy should be introduced.

The main objective of this project is to control the power flow according to the change of load. At first the power of sending end to receiving end is compared from which the power loss of the system is measured. To control the circuit automatically another loop of the line reactance will be introduced which will take care the overall reactance of the system with the change in load or some other fluctuations to meet the power demand.

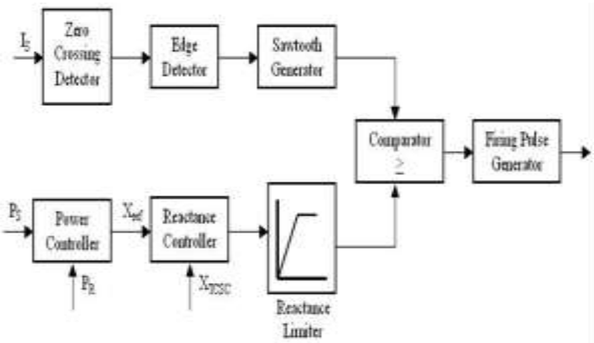


Fig.4. Block Diagram of Control Circuit

The power of sending end $P_{S_{abc}}$ and the receiving end $P_{R_{abc}}$ is compared to generate the error between these two powers (which can be considered as system loss also). The power loop is to be connected to a controller with suitable gain to generate the reference value of the reactance of the line X_{ref} for all the phases. The actual reactance of the device of each phase $X_{A_{TCSC}}, X_{B_{TCSC}}, X_{C_{TCSC}}$ may be generated by dividing the voltage across the device and line current per phase, will be compared with the reference value X_{ref} .

The waveform of the carrier signal is a sawtooth which is generated from the zero crossing of the line current. Since, the line current and its phase angle is totally depends upon the active and reactive power demand of the load connected with the system, the carrier signal is so chosen that it will follow the same phase with the line current. To generate the carrier signal of such type, a Zero Crossing Detector (ZCD) circuit is used that will give a pulse by detecting the phase angle of the line current. The output of the ZCD will connect to an edge detector circuit which may be a differentiator circuit. The edge detector will generate a positive spike during positive edge of the pulse and negative spike during negative edge of the pulse. Using these spikes, a ramp wave can be reset to generate a sawtooth waveform of same supply frequency and same phase angle of the supply current.

After limiting the error signal to a suitable value generated by the reactance loop, the signal is again compared with the carrier signal to generate the firing pulses which will control the overall reactance of the TCSC by the adjustment of firing the thyristors connected in series with the inductor. Since, the generation of the carrier signal is totally load dependent, it will automatically adjust the sequence of firing pulses so that the device will vary the reactance as per the system requirements. The simple block diagram of this control circuit is shown in Fig. 4.

4.1. Design of Outer Power Loop:

As discussed in the previous section, the power loop calculates the difference between the sending end power and the receiving end power.

The sending end voltage and current is measured by connecting a three-phase VI measurement block in the supply side, which will also be used to measure both the sending end active and reactive power and by connecting a three-phase instantaneous active and reactive power measurement block.

Similarly, for the measurement of receiving end voltage and current is measured by connecting another three-phase VI measurement block in the receiving end side, which will also be used to measure both the receiving end active and reactive power and by connecting another three-phase instantaneous active and reactive power measurement block.

Fig. 5 represents the transmission network considering the measurements of sending end and receiving end voltages, currents and active and reactive powers.

The difference between the sending end power and the receiving end power represents the line loss or the error between these two powers. This error signal then connected to a power controller, basically a PI controller which will decide the reference TCSC reactance to be adjusted with the line reactance for controlling the amount of power flow.

4.2. Design of Inner Reactance Loop:

The actual reactance of the TCSC is estimated by dividing the rms voltage across the device and the input current of the device, i.e., line current. Fig.5 shows the measurement of TCSC reactance which is then compared with the reference value of the reactance which is delivered by the power controller.

The error between the reference signal and the actual signal will connect to the reactance controller, which is another PI controller.

The output of the PI controller will generate the modulating signal which is basically a DC signal, compared with a carrier signal. The carrier signal is chosen as sawtooth waveform of magnitude 5V. The modulating signal is limited to a value not more than the value of peak of the sawtooth signal. In this research work, the value of the modulating signal is limited in between 0V to 4.5V.

4.3. Generation of Sawtooth Waveform:

The sawtooth waveform is generated in such a way that it will follow the same phase as line current, which is dependent on the types of load connected in the receiving end and line reactance. Hence, the waveform is to be generated from the line current.

Fig. 6 represents the diagram corresponding to the generation of sawtooth waveform. The line current is compared with a Zero Crossing Detector (ZCD). When the line current is higher than the zero signal, the comparator will generate an output which is a pulse following the same phase angle with the line current. The pulse is connected to a derivative circuit to generate triggering signal of short duration. The signal will be positive during the positive edge of the pulse and negative during negative edge of the pulse.

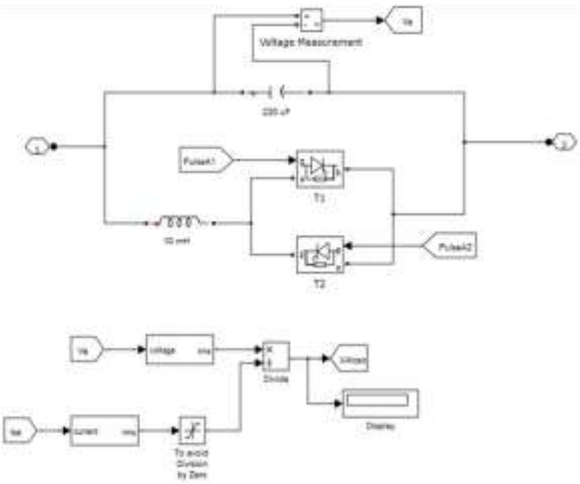


Fig. 5. Measurement of TCSC Reactance

A constant DC signal is required to be integrated to develop a ramp signal which will be reset by the above signal to develop the sawtooth waveform. A suitable gain is applied to maintain the amplitude of sawtooth waveform at 5V, shown in Fig.6.

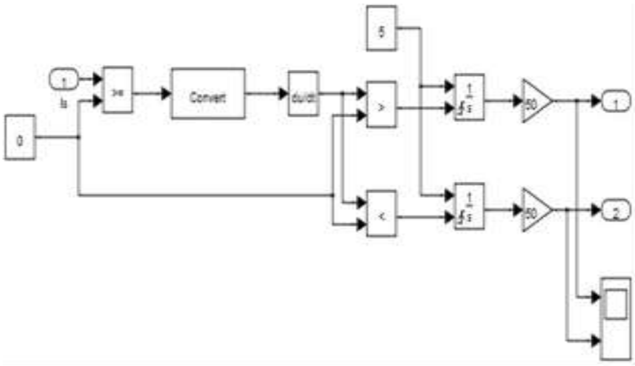


Fig.6. Circuit for generating Carrier Signal

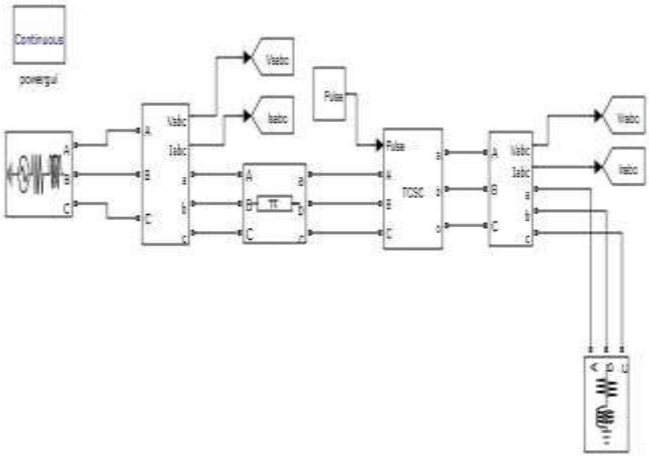


Fig. 7. Simulation Diagram of Three Phase Transmission System

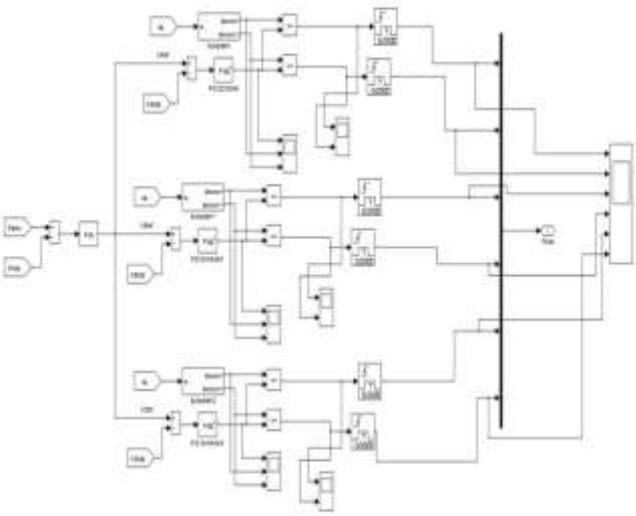


Fig. 8. Detail Control Circuit

5. EXPERIMENTAL RESULTS

The whole control strategy of TCSC has been discussed in the previous section. The transmission line has been checked without connecting the device for various types of loads. Table 1 gives the different parameters measured from the simulation when the line is not associated with the device.

Table 1: Results without TCSC

Sl. No.	Load Data		Load in VA	Sending End Voltage (V)	Without TCSC						Line Loss (Watt)
	Active Power (Watt)	Reactive Power (Var)			Receiving End Voltage(V)	Line Current (A)	Sending End Active Power (Watt)	Receiving End Active Power (Watt)	Sending End Reactive Power (VAr)	Receiving End Reactive Power (VAr)	
1	700	500	860.23	415	397.0	1.12	643.08	640.63	480.93	457.61	2.45
2	750	650	992.47	415	392.1	1.27	672.62	669.45	620.74	580.20	3.17
3	800	600	1000.00	415	393.5	1.29	722.48	719.22	581.67	539.44	3.26
4	1000	800	1280.62	415	386.6	1.63	872.89	867.72	781.12	694.20	5.17
5	1400	1000	1720.47	415	379.0	2.16	1176.65	1167.64	1010.16	834.06	9.01
6	1500	1200	1920.94	415	372.9	2.37	1221.48	1210.60	1188.04	968.52	10.88
7	1800	1200	2163.33	415	371.4	2.67	1455.50	1441.78	1246.46	961.26	13.72
8	1700	1500	2267.16	415	363.7	2.73	1320.04	1305.61	1454.22	1152.04	14.43
9	2000	1200	2332.38	415	370.3	2.87	1608.93	1593.06	1290.95	955.87	15.88
10	2200	1600	2720.29	415	358.5	3.24	1663.03	1642.78	1631.55	1194.79	20.25
11	2300	1800	2920.62	415	353.0	3.43	1686.69	1664.06	1794.18	1302.36	22.63
12	2400	2000	3124.10	415	347.6	3.61	1708.31	1683.21	1951.97	1203.73	25.10
13	2600	2000	3280.24	415	346.4	3.78	1839.88	1812.38	1999.31	1394.19	27.50
14	2800	2600	3820.99	415	331.7	4.22	1822.20	1788.00	2420.85	1660.35	34.20
15	3100	2500	3982.46	415	332.2	4.41	2024.06	1986.73	2434.50	1602.26	37.33
16	3000	2700	4036.09	415	328.4	4.41	1916.27	1878.81	2526.42	1691.00	37.46
17	3400	2800	4404.54	415	324.0	4.76	2117.53	2074.05	2682.72	1708.12	43.48
18	3500	3000	4609.77	415	319.4	4.91	2120.35	2074.08	2817.10	1777.86	46.27
19	4000	3000	5000.00	415	316.6	5.28	2381.21	2327.72	2951.84	1745.86	53.49
20	4200	3000	5161.40	415	315.4	5.43	2481.79	2425.21	3009.50	1732.36	56.58
21	4800	3600	6000.00	415	300.5	6.02	2587.49	2518.00	3464.29	1888.58	69.49
22	5000	4000	6403.12	415	292.5	6.25	2559.96	2484.93	3690.93	1988.06	75.03
23	6000	5500	8139.41	415	264.6	7.19	2540.30	2441.07	4501.19	2237.71	99.23
24	8000	7500	10965.86	415	231.7	8.49	2634.23	2496.00	5504.20	2340.10	138.23
25	10000	7500	12500.00	415	222.4	9.29	3037.84	2872.41	5946.24	2154.39	165.43

Also the line was checked with the same load variations by inserting the device in series with the control mechanism as mentioned the previous section. The same parameters as mentioned in Table 1 is further tabulated as shown in Table 2.

Among the various load data, different waveforms have been taken for a particular load (P=2000W, Q=1800 VAR). Fig. 9 shows the waveforms of the Sending End Voltage, Receiving End Voltage, Sending End Current and Receiving End Current respectively.

To understand the control strategy, control signal for that particular load was also taken. Fig. 10 and Fig. 11 show the control signals and firing pulses respectively.

Under these circumstances, the active powers and the reactive powers both for the Sending End and the Receiving End are also taken as shown in Fig. 12.

Sl. No.	Load Data		Load in VA	Sending End Voltage (V)	With TCSC						Line Loss (Watt)
	Active Power (Watt)	Reactive Power (Var)			Receiving End Voltage(V)	Line Current (A)	Sending End Active Power (Watt)	Receiving End Active Power (Watt)	Sending End Reactive Power (VAr)	Receiving End Reactive Power (VAr)	
1	700	500	860.23	415	414.3	1.17	700.06	697.39	664.80	498.16	2.67
2	750	650	992.47	415	414.1	1.35	750.16	746.60	614.07	647.05	3.56
3	800	600	1000.00	415	414.0	1.36	799.82	796.20	564.19	597.17	3.62
4	1000	800	1280.62	415	413.6	1.48	999.14	993.20	762.54	794.58	5.94
5	1400	1000	1720.47	415	412.9	2.36	1396.32	1385.58	959.60	989.73	10.74
6	1500	1200	1920.94	415	412.6	2.63	1495.97	1482.59	1157.01	1186.11	13.38
7	1800	1200	2163.33	415	412.0	2.97	1792.16	1775.19	1155.82	1183.50	16.97
8	1700	1500	2267.16	415	412.0	3.11	1694.94	1676.32	1452.12	1479.16	18.62
9	2000	1200	2332.38	415	411.9	3.20	1989.26	1969.54	1155.17	1181.76	19.72
10	2200	1600	2720.29	415	411.4	3.73	2187.56	2160.79	1547.70	1571.54	26.77
11	2300	1800	2920.62	415	411.0	4.00	2286.86	2256.04	1743.40	1765.65	30.82
12	2400	2000	3124.10	415	410.7	4.28	2386.25	2351.05	1938.72	1959.26	35.20
13	2600	2000	3280.24	415	410.3	4.49	2582.04	2543.22	1937.26	1956.39	38.82
14	2800	2600	3820.99	415	409.8	5.22	2782.60	2730.14	2521.34	2535.17	52.46
15	3100	2500	3982.46	415	409.9	5.44	3073.85	3016.89	2420.96	2433.04	56.96
16	3000	2700	4036.09	415	409.4	5.52	2978.50	2920.00	2616.58	2628.06	58.50
17	3400	2800	4404.54	415	408.8	6.01	3368.24	3298.72	2709.47	2716.67	69.52
18	3500	3000	4609.77	415	408.6	6.29	3467.34	3391.32	2902.24	2906.92	76.02
19	4000	3000	5000.00	415	407.7	6.82	3950.88	3861.72	2896.83	2896.36	89.16
20	4200	3000	5161.40	415	407.6	7.03	4143.82	4048.90	2894.86	2892.16	94.92
21	4800	3600	6000.00	415	406.2	8.15	4726.76	4599.20	3464.88	3449.52	127.56
22	5000	4000	6403.12	415	405.6	8.69	4923.25	4778.38	3844.88	3822.84	144.87
23	6000	5500	8139.41	415	403.4	10.99	5899.65	5668.15	5251.60	5195.95	231.50
24	8000	7500	10965.86	415	399.4	14.67	7819.35	7407.20	7070.00	6944.48	412.15
25	10000	7500	12500.00	415	396.5	16.61	9657.35	9129.02	7017.50	6846.98	528.33

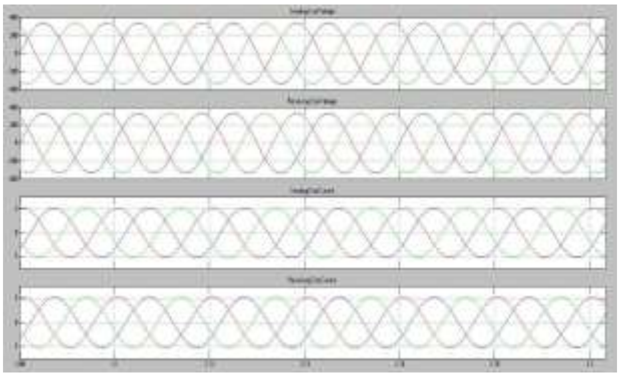


Table 2: Results with TCSC

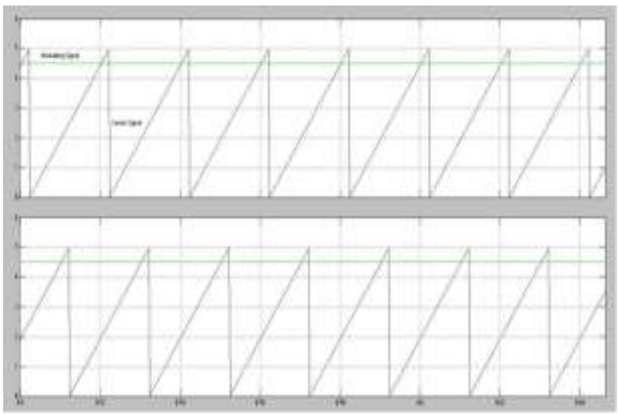


Fig. 9. Sending End Voltage, Receiving End Voltage, Sending End Current and Receiving End Current

Fig. 10. Modulating Signal and Carrier Signal

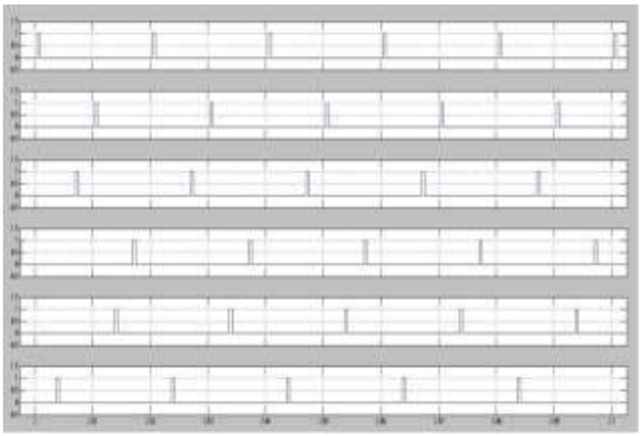


Fig. 11. Firing Pulse for the Thyristors

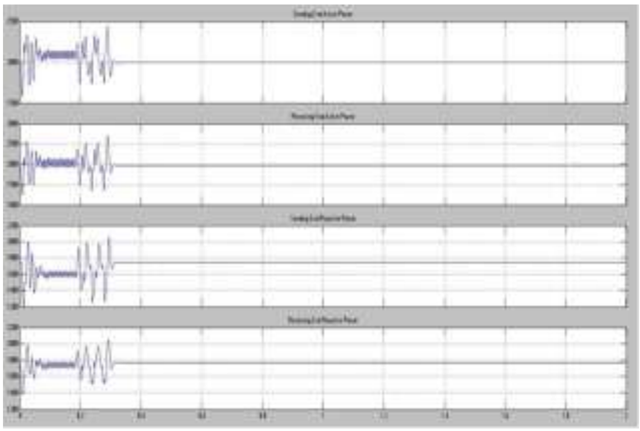


Fig. 12. Sending End Active Power, Receiving End Active Power, Sending End Reactive Power and Receiving End Reactive Power

6. DISCUSSIONS

A comparative study of the voltage regulations and the line efficiency is given in Table III for the above loads. It is evident from Table 3 that the voltage regulation using TCSC is much improved for heavier loads. But it is seen from the table that the line efficiency remains same, so that by using the TCSC, line efficiency will not be affected. Also due to increase in load voltage, load power will also increase and as a result increased line current will cause the increased line loss. Table III shows that line efficiency will remain same regardless the increase of line loss.

Fig. 13 shows the change in line current after using TCSC. Since, the load voltage as well as load power will increase, the line current will also increase and Fig. 14 shows the corresponding line loss.

Table 3: Comparative Results of % Voltage Regulation and % Efficiency

Sl. No.	Without TCSC		With TCSC	
	% Voltage Regulation	% Efficiency	% Voltage Regulation	% Efficiency
1	4.53%	99.62%	0.17%	99.62%
2	5.84%	99.53%	0.22%	99.53%
3	5.46%	99.55%	0.24%	99.55%
4	7.35%	99.41%	0.34%	99.41%
5	9.50%	99.23%	0.51%	99.23%
6	11.29%	99.11%	0.58%	99.11%
7	11.74%	99.06%	0.73%	99.05%
8	14.11%	98.91%	0.73%	98.90%
9	12.07%	99.01%	0.75%	99.01%
10	15.76%	98.78%	0.88%	98.78%
11	17.56%	98.66%	0.97%	98.65%
12	19.39%	98.53%	1.05%	98.52%
13	19.80%	98.51%	1.10%	98.50%
14	25.11%	98.12%	1.27%	98.11%
15	24.92%	98.16%	1.24%	98.15%
16	26.37%	98.05%	1.37%	98.04%
17	28.09%	97.95%	1.52%	97.94%
18	29.93%	97.82%	1.57%	97.81%
19	31.08%	97.75%	1.79%	97.74%
20	31.58%	97.72%	1.82%	97.71%
21	38.10%	97.31%	2.17%	97.30%
22	41.88%	97.07%	2.32%	97.06%
23	56.84%	96.09%	2.88%	96.08%
24	79.11%	94.75%	3.91%	94.73%
25	86.60%	94.55%	4.67%	94.53%

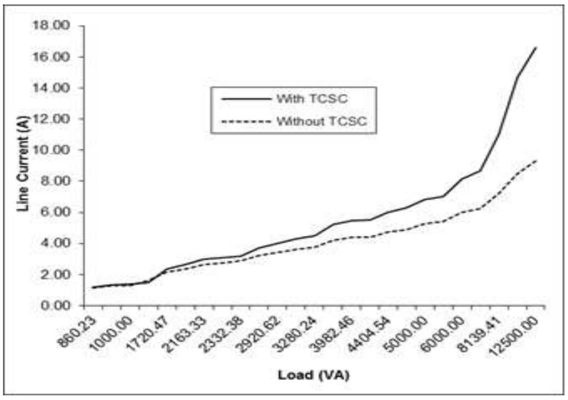


Fig. 13. Load vs Line Current

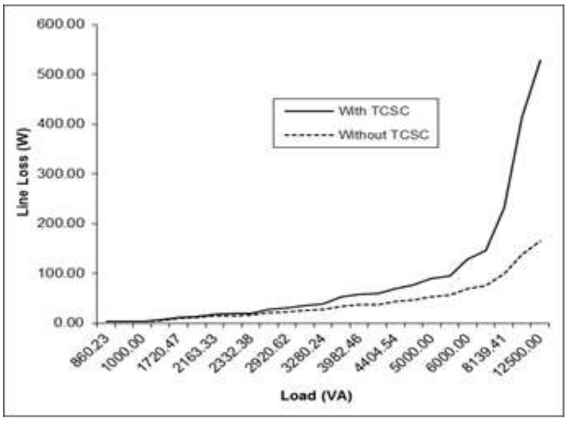


Fig. 14. Load vs Line Loss

The receiving end voltage with and without the device and corresponding voltage regulation are shown in Fig. 15 and Fig. 16 respectively. It is evident from both the Fig.s that the receiving end voltage and the corresponding line regulation can be increased by using the device.

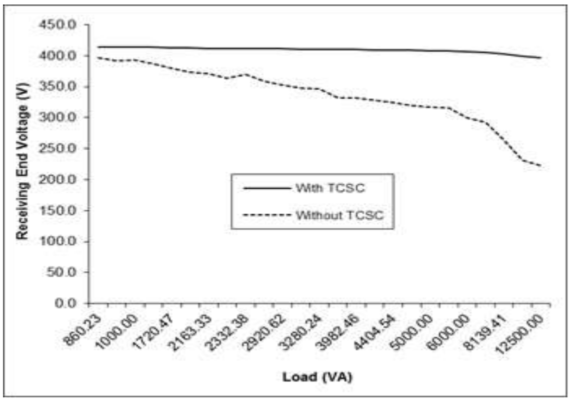


Fig. 15. Receiving End Voltage

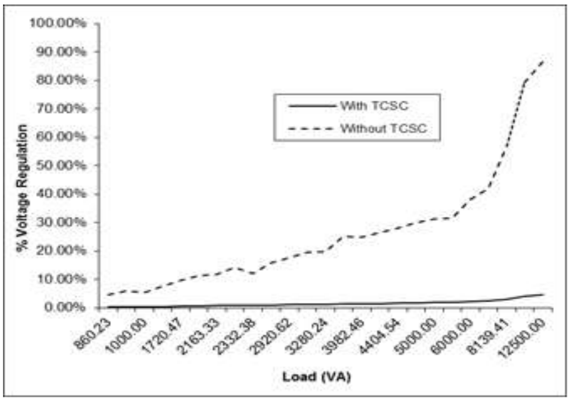


Fig. 16. Line Voltage Regulation

REFERENCES

[1] S. Meikandasivam, R. K. Nema, S. K. Jain, "Behavioral Study of TCSC Device – A MATLAB/Simulink Implementation", World Academy of Science, Engineering and Technology 45 2008.

[2] D. Jiang, X. Lei, "A nonlinear TCSC control strategy for power system stability enhancement", Proceedings of the 5th International Conference on Advances in Power System Control, Operation and Management, AFSCOM 2000, Hong Kong, October 2000.

[3] Hu Zhen_da, Dai Chao_bo, Wu Shou_yuan "A Pilot Study of a Novel TCSC Scheme for the UHV Transmission Lines", 978-1-4577-0547-2/12/$31.00 ©2012 IEEE.

[4] E.A. Leonidaki, N.D. Hatziargyriou, B.C. Papadias, G. J. Georgantzis, "Investigation of Power System Harmonics and SSR phenomena related to Thyristor Controlled Series Capacitors", Paper accepted for presentation at the 8th ICHQP '98, jointly organized by IEEE/PES and NTUA, Athens, Greece, October 14-16, 1998.

[5] N .G .Hingorani, Laszlo Gyugyi, "Understanding FACTS", IEEE Press, 2001, pp 223-238.

[6] S. Jahdi, L. L. Lai, "Affects of TCSC Usages on Distance Protection and Voltage Profile of a System; A Novel", 978-1-4577-1250-0/11/$26.00 ©2011 IEEE.

[7] V. Mahajan, "Thyristor Controlled Series Compensator", 1-4244-0726-5/06/$20.00 '2006 IEEE, pp. 182-187.

[8] B. S. Rigby, "An AC Transmission Line Power Flow Controller using a Thyristor Controlled Series Capacitor", IEEE Africon 2002, pp. 773-778.

[9] A.Ally, B. S. Rigby, "An Investigation into the Impact of a Thyristor Controlled Series Capacitor-Based Closed-Loop Power Flow Controller under Fault Conditions", IEEE Africon 2004, pp. 675-681.

[10] M. H. Abardeh, J. Sadeh, "Effects of TCSC Parameters and Control Structure on Damping of Sub-Synchronous Resonance", The 4th International Power Engineering and Optimization Conf. (PEOCO2010), Shah Alam, Selangor, MALAYSIA: 23-24 June 2010, pp. 26-32.

[11] W. Shouyuan, Z. Xiaoxin, L. Yajian, "Design and Simulation on TCSC Analog Model And Controller", 0-7803-4754-4/98/$10.00 © 1998 IEEE, pp. 430-435.

[12] Z. Xueqiang, "Study of TCSC Model and Prospective Application in the Power Systems of China", IEEE 1999 International Conference on Power Electronics and Drive Systems, PEDS'99, July 1999, Hong Kong, pp. 688-691.

[13] A.H. Li, Q. H. Wu, P. Y. Wang, X. Zhou, "Influence of the Transient Process of TCSC and MOV on Power System Stability", IEEE Transactions On Power Systems, Vol. 15, No. 2, May 2000, pp. 798-803.

[14] A. Ghosh, A. Joshi, M. K. Mishra, "State Space Simulation and Accurate Determination of Fundamental Impedance Characteristics of a TCSC", IEEE Power Engineering Society Winter Meeting, 2001, pp. 1099-1104.

[15] H. S. Sun, S. Cheng, J. Wen, "Dynamic Response of TCSC and Reactance Control Method Study", 2006 International Conference on Power System Technology, pp. 1-5.

[16] S. A. Zaid "Thyristor Firing Circuit Synchronization Techniques in Thyristor Controlled Series Capacitors", 978-1-4244-8930-5/11/$26.00 ©2011 IEEE, pp. 183-188.

[17] D. Chatterjee A. Mitra S. Sarkar, "A Conceptual Study for Control Strategy of TCSC in Inductive and Capacitive Region", 2014 International Conference on Circuit, Power and Computing Technologies [ICCPCT], pp. 1-6.