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Binary Phase Shift Keying Demodulation & its Simulation on MATLAB

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Abstract: This paper describes about BPSK demodulation using costas loop and implementing on a DSP kit. Carrier recovery is done using a costas loop which requires a PLL. PLL contains a phase detector, VCO and a LPF which are simulated in MATLAB. Costas loop contains two PLLs which are in quadrature with each other. The BPSK modulation by representing binary data by different phases of a sinusoidal signal and demodulation by using Costas loop is implemented on MATLAB. The MATLAB codes are written to plot the various graphs for input, error voltage and VCO frequency and the demodulated output for the digital binary data taken from the user.

Keywords: BPSK demodulation, Costas Loop, Phase locked loop.

1. Introduction

In the earlier days in satellite communication analog systems were used for the communication between the base station and the satellite, but there were many disadvantages of using the analog systems for satellite communication. The incorporation of the analog system for communication occupied large area on the satellite up to few square feet. This would in turn lead to more consumption of the fuel which was not preferred. This lead to the use of digital systems for communication [6].
The advantages of the digital systems are, they are less expensive, more compatible, easy to manipulate, flexible, compatible with other digital systems, transmission without degradation and integral network.
These advantages lead to use of digital systems in satellite communication. There are different techniques of digital modulation namely ASK (Amplitude shift keying), FSK (frequency shift keying), PSK (phase shift keying), QPSK (quadrature phase shift keying), MSK (minimum shift keying), but for satellite communication the BPSK is employed the reason behind that is communication between the base station and the satellite is small commands in which the data rate is less of around 4Kbps , hence the BPSK type of modulation and demodulation is employed. BPSK is preferred over FSK because FSK causes Doppler shift, it uses high speed transmission and less efficient in both power and bandwidth [7].

2. THE NEED FOR PHASE LOCKED LOOP (PLL)

Whenever digital data are transmitted by band pass modulation, synchronization on different signal levels will be required. When binary phase shift keying (BPSK) is used to modulate the phase of carrier, the receiver must be able to perform demodulation synchronously, that is the receiver generates the replica of the carrier and multiplies the incoming signal with the reconstructed carrier. This shifts the spectrum of the received signal by a frequency offset which is equal to the carrier frequency and the data signal is obtained by simple low pass filtering. Because the replica of the carrier must be in phase with the data signal, phase synchronization is required. PLL's are made use of not just in data transmission but also for recording, the disturbances and vibrations caused by the various instruments in the satellites.[1,2,3]

3. The Need for Phase Shift Keying

Development during the earlier days of deep space programs, phase shift keying now finds widespread use in both military and commercial communication systems. For telemetry applications, PSK is considered an efficient form of data modulation because it provides the lowest probability of error for a given received signal level, when measured over one symbol. Terrestrial microwave radio links and satellite communication systems also frequently employ PSK as their modulation format.

Binary Phase Shift Keying (BPSK), in terms of noise immunity per bandwidth, is one of the most efficient binary data modulation techniques. Yet, communication systems designers often neglect this option because the design of a BPSK demodulator is not as mathematically simple or straight forward as frequency shift keying (FSK). the prospect of having to apply through engineering knowledge to design a BPSK demodulator can be daunting. However it is unlikely that any such circuit will perform as well as it could if it were implemented without fully understanding and parameterizing it behavior.

4. The necessity of a Digital signal processor

There are various ways in which a PLL or a demodulation circuit can be implemented. It is not practical to build a whole

analog system because it becomes difficult to predict how each and every component will behave in the extreme conditions when they are put into space orbits, furthermore the complexity of the unit increases when there are many components. It is therefore convenient to build the whole thing in one chip. This can be done using either microprocessors, CPLD's, FPGA's or Digital signal processors. Microprocessors are not quite capable of performing real time operations on signals for it requires a lot of complex mathematics.[4] Even though CPLD's and FPGA's performance is satisfactory and being extensively used for various processes in Space research Organization, it is not wise to make use of these expensive chips to implement a small algorithm. Furthermore, software development and trouble shooting is simpler in DSP. It was therefore decided to implement the process using a Digital Signal Processor.[5,9]

5. Experimental Procedure

PLL is required to lock the low frequency disturbances that are caused in a satellite. Most of the simulations and software implementations are done using low frequencies from 3-10KHz. The first step in the project was to design a PLL.[10] These blocks are implemented in the ADSP 21020 using C. After referring to some papers presented by the scientists, a costas loop was constructed as a demodulator [8]. A considerable time was spent for studying the processor, the science of processing and deriving the design equations. The processor was used has a maximum sampling rate of 44KHz. Hence various design equations were derived.

6. Binary Phase Shift Keying

BPSK consists of shifting the phase of a sinusoidal carrier 0 deg or 180 deg with a uni-polar binary signal. It is equivalent to PM signaling with a digital waveform and is also equivalent to modulating a DSB-SC(double side band suppressed carrier) signal with a polar digital waveform.[11].

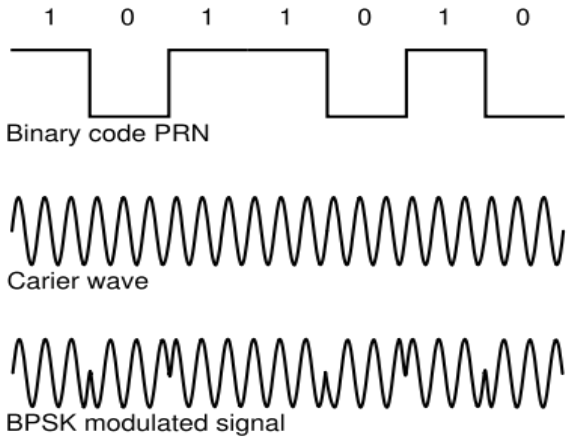

Figure 1 : BPSK Modulation

The resulting transmitted BPSK is

$$S(t) = \begin{Bmatrix} A\cos(2\pi f_c t) \\ A\cos(2\pi f_c t+\pi) \end{Bmatrix} = \begin{Bmatrix} +A\cos(2\pi f_c t) & \text{binary 1} \\ -A\cos(2\pi f_c t) & \text{binary 0} \end{Bmatrix} \quad (1)$$

f_c is the carrier frequency

Because a phase shift of 180^0 (π) is equivalent to flipping the sine wave or multiplying it by -1, this leads to a convenient formulation. d(t) can be assumed to be a discrete function that takes sample values of +1 and -1 for the corresponding bits 1 and 0s.
Equation 1 can be rewritten as

$$S_d(t)=A\, d(t)\cos(2\pi f_c t) \quad (2)$$

7. Performance Characteristics of PSK

In order to study the performance of various schemes, the first parameter taken into consideration is the bandwidth of the modulated signal. This depends on a variety of factors, including the definition of the bandwidth used and the filtering techniques used to create the band pass signal.

8. Multilevel PSK

With the multilevel PSK, significant improvements in bandwidth can be achieved. In general,

$$B_r = \left[\frac{1+r}{L}\right] R = \left[\frac{1+r}{\log_2 M}\right] R \quad (3)$$

Where, R is the bit rate, R is related to the technique by which the signal is filtered to establish a bandwidth for transmission , L is the number of bits encoded per signal element and M is the number of different signal elements.
DPSK and BPSK are about 3dB superior to ASK and BFSK. The error probability for a given value E_b/N_0 (E_b is the signal energy per bit and N_0 is the noise power density per hertz) increases as M increases but the bandwidth efficiency of MPSK increases an M increases.[12]

Table 1: Data rate to transmission BW Ratio for various schemes

The table above shows the ratio of data rate, R , to transmission bandwidth for various schemes.
This ratios is also referred to as bandwidth efficiency.

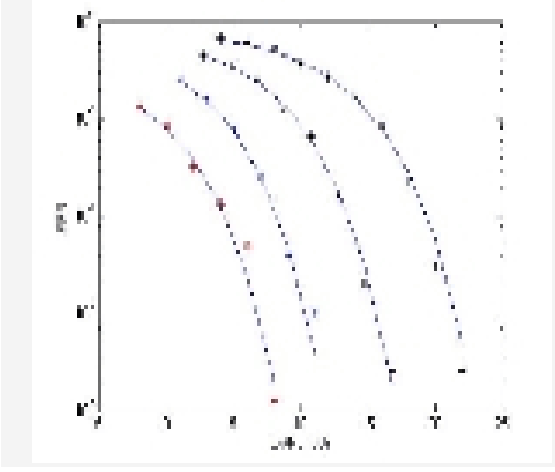

Figure 2.1 : BER Chart for Multilevel PSK

	r=0	r=0.5	r=1
Phase Shift Keying	*1.0*	*0.67*	*0.5*
Multilevel Keying			
M=4, L=2	*2.00*	*1.33*	*1.00*
M=8. L=3	*3.00*	*2.00*	*1.50*
M=16, L=4	*4.00*	*2.67*	*2.00*
M=32, L=5	*5.00*	*3.33*	*2.50*

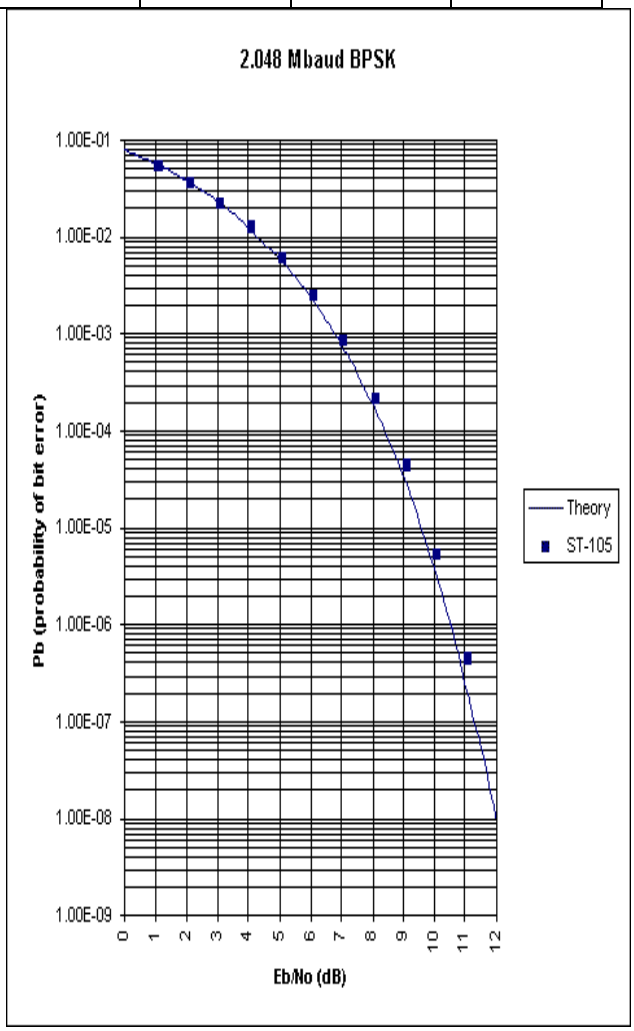

Figure 2.2 : BER Chart for BPSK

9. MATLAB IMPLEMENTATION

MATLAB is a computer program that can be very helpful in solving the sorts of mathematical problems you will frequently encounter throughout your engineering or technology coursework. We can use built-in features of MATLAB to effortlessly solve a wide variety of numerical problems, from the very basic, such as a system of 2 equations with 2 unknowns:

X+2Y=24
12X - 5Y = 10

to the more complex, such as factoring polynomials, fitting curves to data points, making calculations using matrices, performing signal processing operations such as Fourier transforms, and building and training neural networks. A very powerful and often very useful aspect of MATLAB is that it can be used to plot many different kinds of graphs, enabling you to visualize complex mathematical functions and laboratory data.

9.1 Matlab implementation of BPSK demodulation

The code first performs the modulation of the digital data by representing the binary 1 data by positive going sine wave signal and binary 0 by a negative going sine wave signal. The demodulation is done by determining the phase difference between the input signal and the oscillations produced by the frequency oscillator. Then this error signal is used to lock the vco frequency and phase to the incoming modulated signal. The obtained output waveform for the digital data taken from the users are shown in the following screenshots.

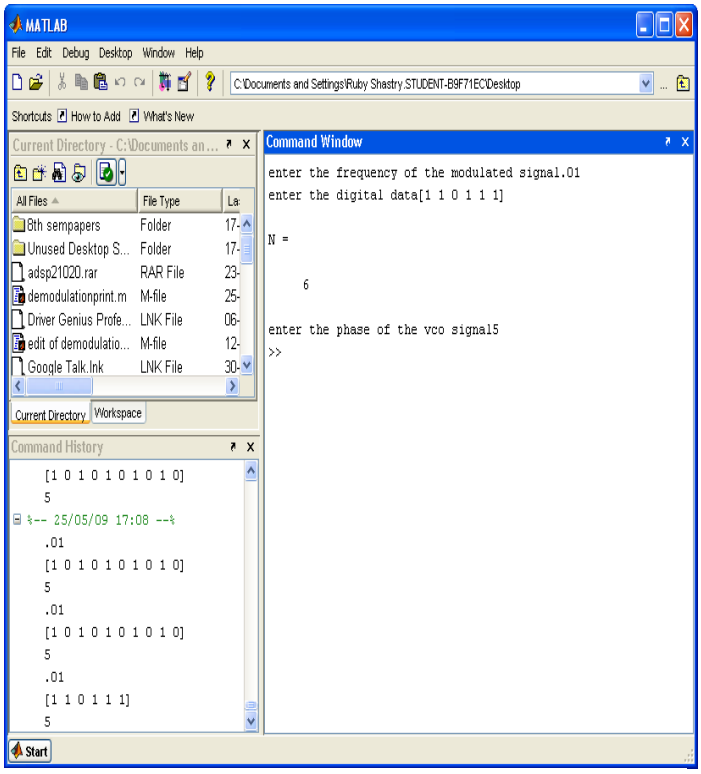

Figure 3.1: Input data

The figure 3.1 shows the screenshot of Matlab command window where the digital input data stream is given by the user with the modulate frequency as well the phase of the VCO signal. The fvco frequency is generated in the program. The figure 3.1 shows the input digital data given as [1 1 0 1 1 1].The figure 3.2 shows the corresponding Binary Phase shift

modulate signal with phase shift occurring at the transition from 1 to 0 and 0 to 1.

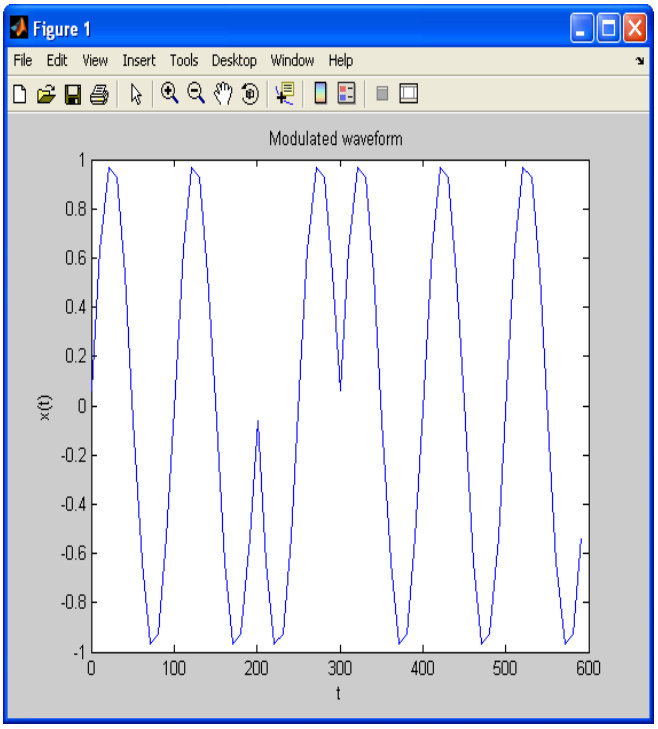

Figure 3.2: Modulated BPSK

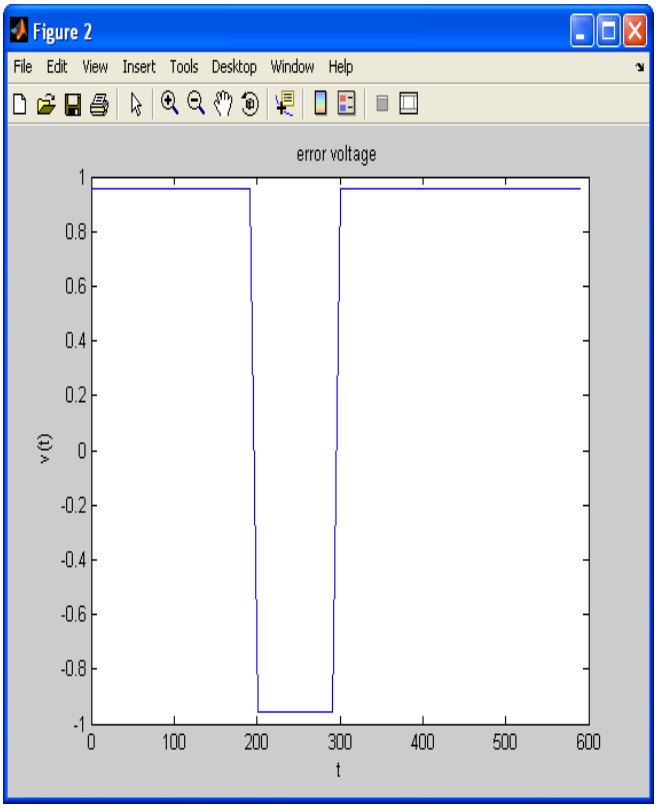

Figure 3.3: Error voltage

Figure 3.3 shows the DC error voltage obtained due to the phase difference between the modulated signal and the VCO signal. This error is given as a feedback to generate the VCO signal such that the phase difference between the modulated signal and the VCO signal is zero.

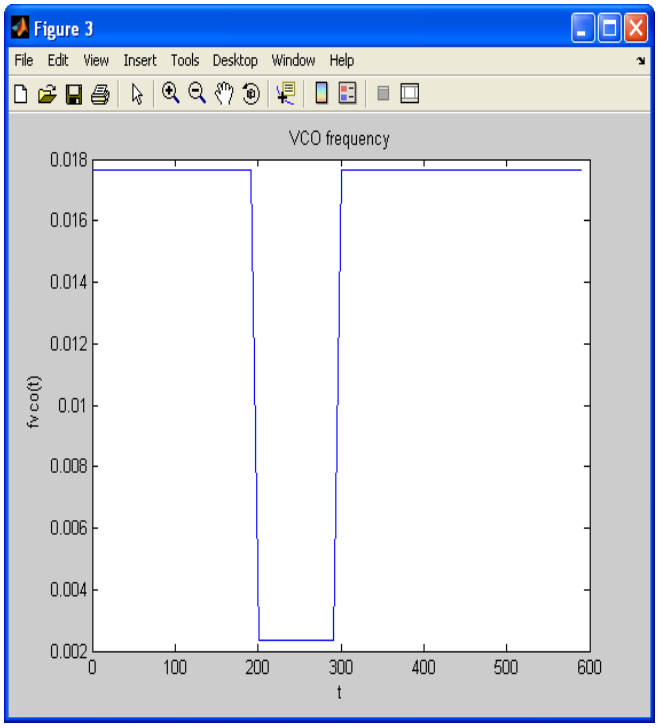

Figure 3.4: Value of the new VCO frequency

Fig 3.4 shows the value of the new frequency of the VCO signal generated to overcome the phase error so that the phase of the VCO signal gets locked to the phase of the modulated signal.

Figure 3.5 shows the demodulated output. Once the signal gets locked to incoming modulated signal the output of this is fed to the in phase and quadrature PLL blocks where the decision devices extract the corresponding bits from the waveforms by making use of clock recovery circuits.

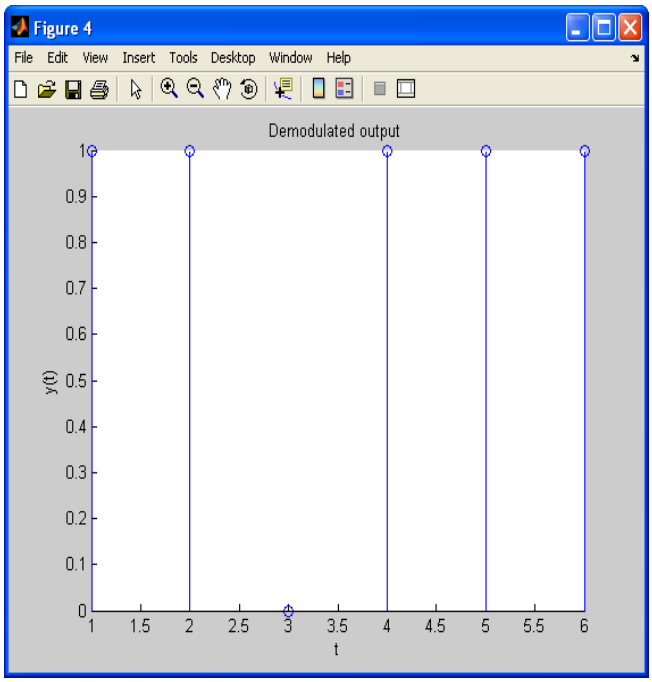

Figure 3.5: Demodulated output

10. Conclusion

A lot of thought, research and experimentation has gone into this project. There is no such thing as an ideal design, further modifications can be done to this project to improve its performance. For any assignment a basic foundation is necessary and this is what we have tried to achieve in this venture. Costas demodulation loop has been successfully implemented using ADSP 21062 processor. By making slight modifications of the design equations it is possible to use the same program for real time high quality demodulation purpose. The focus of this project does not lie in merely implementing some concept, but rather in studying the various ways in which it can be implemented.

11. Future Scope of the Project

BPSK modulation and demodulation is used for a low data transmission of commands from the base station to the satellite system. Also there is sometimes phase ambiguity at the receiver. So for transmitting any information at a higher data rate and in order to improve the overall efficiency, it can be extended to Quadrature Phase Shift Keying (QPSK) in which two bits can be represented using a single phase of the carrier. The error rates of both BPSK and QPSK are same. In QPSK the bandwidth requirement is half as that of BPSK and data rate is twice. Also this can be extended to M-array modulation in which M bits are represented using one phase of the carrier thus reducing the bandwidth requirement.

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