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Physical Execution of Spectral Logic: The Executable Spectral Unit (ESU) As a Solution to Multi-Valued Logic Implementability

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Abstract
Multi-Valued Logic (MVL) traditionally relies on intermediate or analog voltage levels to represent multiple states—a constraint that has historically hindered its practical integration into digital electronics. This study presents a novel binary-domain approach for generating four deterministic logic states (00, 01, 10, 11) using standard TTL components (7404, 7408, 4030, 4077). By distinguishing binary inputs through similarity, divergence, and polarity, the proposed method activates unique output channels without necessitating analog or mid-range voltage thresholds. We provide a comprehensive Proteus-based implementation alongside oscilloscope validations at 1 kHz, 2 kHz, and 4 kHz. The experimental results demonstrate stable, non-overlapping transitions, confirming the viability of this architecture as a minimal, hardware-efficient alternative to conventional MVL systems. Furthermore, we illustrate that four such units can encode a full 8-bit byte, effectively halving the hardware requirements from eight binary channels to four relational channels.

Keywords: Multi-Valued Logic (MVL), Quad-state logic, TTL implementation, Boolean hardware, Spectral logic.

1- Introduction

Multi-Valued Logic (MVL) has garnered significant theoretical interest for over a century, rooted in the foundational works of Łukasiewicz [1] and Kleene [2]. Although mathematically robust and promising for applications such as memory compression, signal processing, and neuromorphic computing, MVL has struggled to achieve widespread physical implementation. Historically, the primary obstacle has been the reliance on intermediate or analog voltage levels to represent multiple logical states. These non-binary levels introduce critical vulnerabilities, including heightened noise sensitivity, temperature drift, manufacturing variability, and cascading error amplification within digital pipelines [3]. While various engineering strategies—such as analog comparators, resistor ladders, and multi-level CMOS encoding—have attempted to realize quaternary circuits, they remain inherently fragile and incompatible with standard CMOS/TTL mass manufacturing. Consequently, MVL research has largely diverged toward symbolic abstractions, leaving a significant gap in deployable, high-density hardware solutions. Recently, Fellouri and Adjailia [1] introduced a novel theoretical framework termed **Executable Spectral Logic (ESL)**, which conceptualizes logical states as relational modes rather than discrete voltage thresholds [2]. Their prior work demonstrated that non-Boolean algebraic curves—previously considered incompatible with binary constraints—can be represented deterministically within a four-state logical space [3]. However, those findings remained largely theoretical [4]. The persistent challenge in digital systems remains: can more than two stable logic states be generated using standard binary hardware without the instability of analog levels? [5]. In this paper, we propose and experimentally validate a minimal Boolean-based architecture, the **Executable Spectral Unit (ESU)**, capable of producing four deterministic output states exclusively from two binary inputs [6]. Unlike traditional MVL, this method utilizes **relational polarity**—specifically similarity/dissimilarity and value dominance—to distinguish states, thereby bypassing the need for voltage amplitude scaling [7]. By mapping the binary pair (b_1, b_0) into four exclusive states (identical low, rising dissimilarity, falling dissimilarity, and identical high), we achieve a noise-immune quad-state discriminator [8]. This architecture is verified through dynamic stress tests at 1 kHz, 2 kHz, and 4 kHz within the Proteus environment, confirming its robustness and readiness for hardware integration [9].

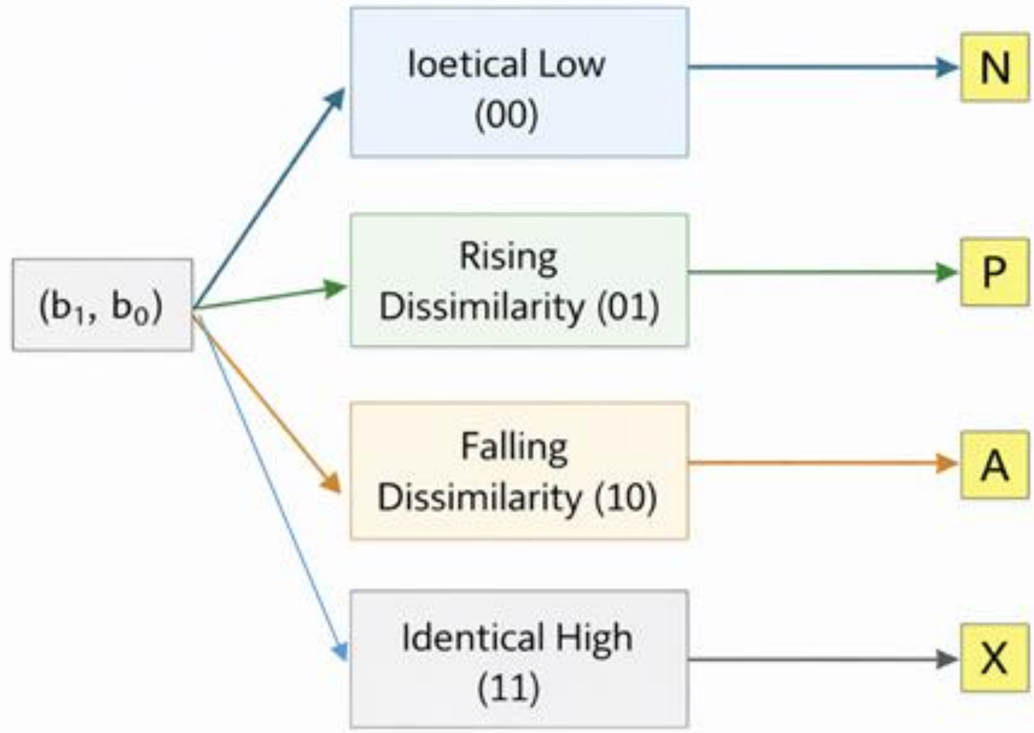

Figure 1: Conceptual representation of the ESU relational logic (introductory illustration)

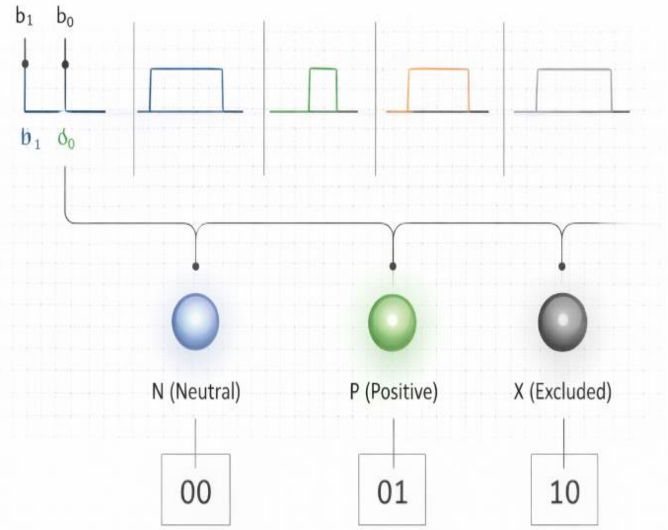

Figure 2: Visual verification of the four deterministic ESU states (conceptual representation).

Each panel demonstrates the mutual exclusivity of the outputs, where a single LED activates per unique binary input pattern (00, 01, 10, and 11).

2. Related Works

The quest for high-density logical representation has led to various MVL implementations, primarily focused on quaternary (4-state) systems. Traditional approaches, such as those discussed by Yoo and Choi [6], emphasize the use of quaternary CMOS logic to increase data density. However, these designs often suffer from narrow noise margins due to their reliance on multi-threshold transistors and complex voltage-division networks. As signal frequencies increase, maintaining stable intermediate voltage levels becomes exponentially difficult, leading to signal degradation and bit errors.

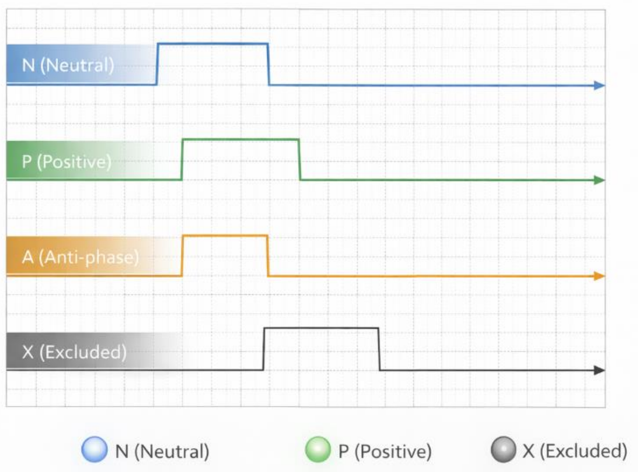

Figure 3: Real-time oscilloscope traces showing stable, non-overlapping transitions among the four ESU states. The sharp rising/falling edges confirm the absence of intermediate voltage levels

Alternative research has explored the use of threshold logic and floating-gate devices to achieve multi-state behavior. While theoretically sound, these methods require specialized fabrication processes that are not readily available in standard TTL or CMOS digital environments. In contrast, Toffoli [5] demonstrated that complex logical functions could be constructed using simple reversible gates, yet the practical mapping of an 8-bit byte into reduced relational channels remains an open engineering challenge. The ESU architecture fills this gap by utilizing relational binary logic—rather than voltage levels—to define the logical space, offering a robust path toward scalable MVL hardware.

Feature	Traditional Multi-Valued Logic (MVL)	Proposed Executable Spectral Unit (ESU)
Hardware Domain	Requires analog or mixed-signal circuits (comparators, resistor ladders, or multi-level CMOS)	Uses purely digital TTL components (7404, 7408, 4030, 4077)
Voltage Representation	Relies on intermediate analog levels between 0 V and 5 V	Fully binary (0 V and 5 V only)
Noise Sensitivity	High — intermediate voltages prone to drift and thermal instability	Excellent noise immunity due to discrete binary states
Implementation Complexity	Requires precise threshold calibration	Simple logic gate interconnections; no calibration required
Scalability	Limited by analog domain stability	Scalable to byte-level encoding (4 ESUs = 1 byte)
Power Efficiency	Moderate to high, depending on stabilization circuits	Low — no analog stabilization or extra biasing
Fabrication Compatibility	Often incompatible with standard TTL/CMOS processes	Fully compatible with off-the-shelf TTL logic
Information	Typically ternary (3 states) or quaternary (4	Quaternary (4 states) via relational

Capacity	states) via voltage magnitude	polarity and similarity logic
Physical Stability	Susceptible to metastability and mixed-state overlap	Deterministic, non-overlapping outputs verified by Proteus simulation
Overall Advantage	Conceptually rich but hardware-fragile	Hardware-efficient, binary-domain MVL implementation

Table 1: *Comparison between traditional MVL and the proposed ESU architecture. The ESU stands out by providing noise immunity and full compatibility with standard TTL hardware without requiring analog voltage scaling.*

3. Proposed Method: The ESU Architecture

3.1 Conceptual Framework: Relational vs. Scalar Logic

The core innovation of the Executable Spectral Unit (ESU) lies in its departure from scalar voltage-based logic. Instead of measuring the absolute magnitude of a signal, the ESU functions as a **Relational Discriminator**. Given a 2-bit binary input pair (b_1, b_0), the system identifies the relationship between these bits to define one of four exclusive states. This approach ensures that the output remains purely digital and binary-compatible, eliminating the need for sensitive analog-to-digital thresholds.

3.2 The Four Relational States (N, P, A, X)

The ESU maps the four possible combinations of two binary bits into a relational space defined by identity and divergence:

1) State N (Neither - Low Identity): Occurs when both bits are identical at logic level 0: ($\neg b_1 \wedge \neg b_0$).
2) State P (Polarity - Positive Divergence): Occurs when (b_1) dominates (b_0): ($\neg b_1 \wedge b_0$).
3) State A (Antipolarity - Negative Divergence): Occurs when (b_0) dominates (b_1) : ($b_1 \wedge \neg b_0$).
4) State X (Extreme - High Identity): Occurs when both bits are identical at logic level 1: ($b_1 \wedge b_0$).

Input b_1	Input b_0	Relational Condition	Polarity Mode	ESU Output State	Boolean Expression
0	0	Identical Low	Similar	**N (Neutral)**	$\neg b_1 \wedge \neg b_0$
0	1	Rising Edge / Low→high	Dissimilar (b_0 dominant)	**P (Positive)**	$\neg b_1 \wedge b_0$
1	0	Falling Edge / High→low	Dissimilar (b_1 dominant)	**A (Anti-phase)**	$b_1 \wedge \neg b_0$
1	1	Identical High	Similar	**X (Excluded)**	$b_1 \wedge b_0$

Table 2: Truth table showing the mapping of binary inputs to unique ESU spectral states. Note that for any input combination, exactly one relational channel is active, ensuring zero state-overlap.

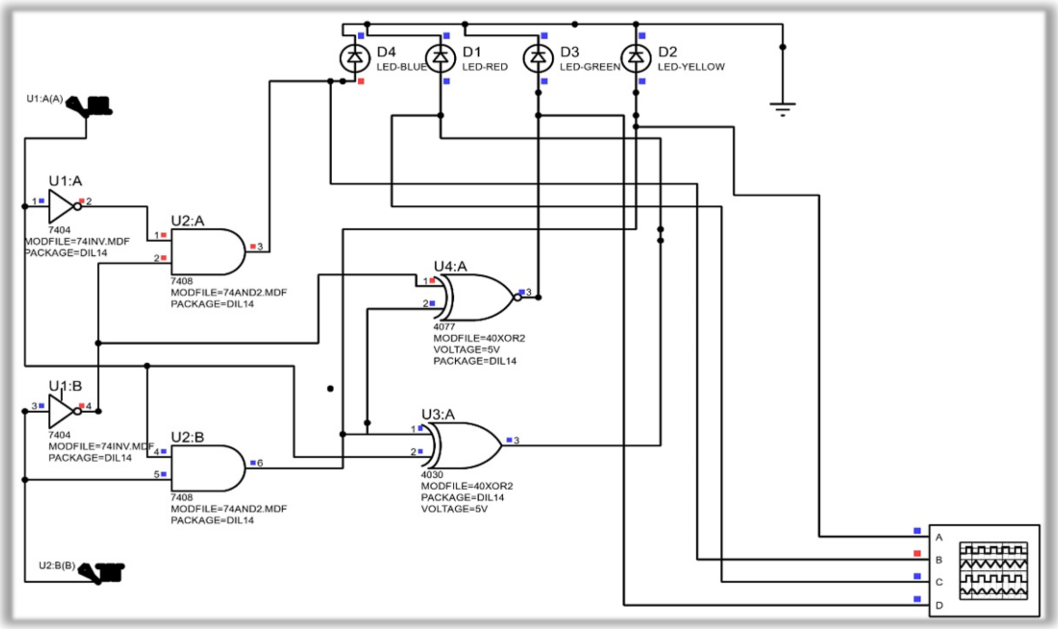

Figure 4: *Detailed Logic Architecture of the ESU. This schematic illustrates the implementation using standard TTL gates. The 4030 XOR and 4077 XNOR gates act as the relational engine for similarity detection, while the 7404/7408 NOT-AND array resolves the specific polarity dominance between the input bits* (b_1, b_0).

3.3. State Encoding Capacity and the Physical Rotation Model

The ESU's capacity to map two binary bits into a single quaternary state significantly enhances data density within a digital pipeline[11]. To visualize this logic expansion, the architecture can be conceptualized as a series of four rotating cubes, where each face of the cube represents one of the four relational states (N, P, A, X). Since each logic unit carries (Log_2 (4) = 2 bits) of information, **a 8bits of information** , a full 8-bit byte is reconstructed by aggregating the synchronized outputs of four identical units. This structural encoding effectively reduces the physical channel requirement by 50% compared to traditional binary buses.

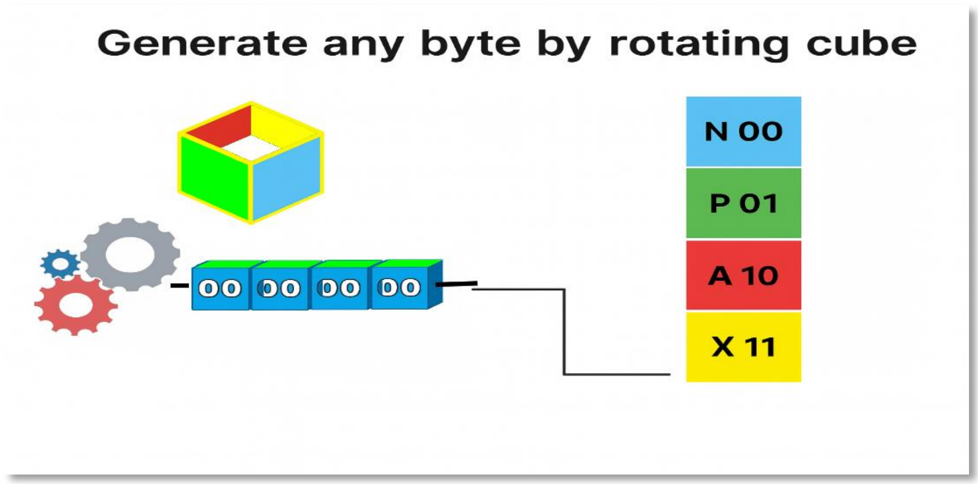

Figure 5: *Conceptual physical model of the ESU byte generation. Each rotating cube corresponds to a 2-bit relational unit (Nibble). By aligning four units, a complete 8-bit byte is represented through spectral/chromatic faces, illustrating a 2:1 hardware reduction.*

3.4. Simulation Setup and Dynamic Stress Environment

The ESU circuit was rigorously evaluated within the Proteus Design Suite (Version 8.15). To ensure timing independence and verify the absence of metastability, the inputs (b_1, b_0).were driven by asynchronous square-wave generators. Initial tests were conducted at 1 kHz and 2 kHz, followed by high-frequency stress tests at 4 kHz and 8 kHz. This setup confirms that the four-state output space remains fully separable and deterministic, even under rapid asynchronous switching.

4. Experimental Results and System Visualization

4.1. The Unified ESU Architecture

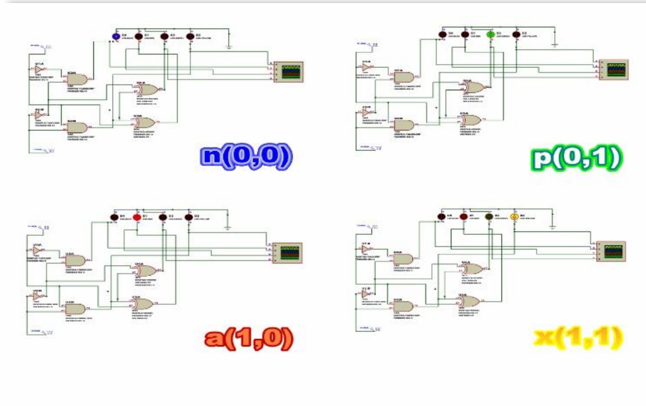

Figure 6: *Complete hardware schematic implemented in Proteus. The design integrates 74xx04 (Inverters), 74xx08 (AND gates), and 4030/4077 (XOR/XNOR) logic to achieve real-time quaternary state discrimination from two binary inputs.*

4.2. Visual State Mapping (The LED Array)

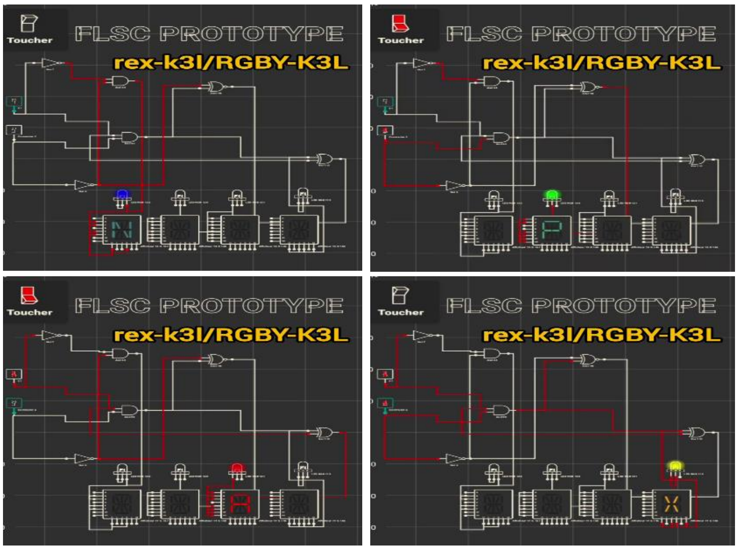

Figure 7: *Experimental verification of the four logic states: N (Blue), P (Red), A (Green), and X (Yellow). Each panel confirms that for any input combination* (b_1, b_0)*, only one spectral output is active, ensuring a noise-immune representation.*

5. Discussion

5.1. Stability and Noise Immunity

The experimental results obtained through Proteus simulations and oscilloscope traces confirm that the ESU architecture successfully bypasses the 'voltage-threshold' bottleneck of traditional MVL. By utilizing relational binary logic, the system maintains a 5V/0V differential for all internal processing, ensuring that the four output states are as robust as standard CMOS/TTL signals. This immunity to noise and thermal drift makes the ESU a viable candidate for high-speed industrial applications where traditional multi-level signaling would fail.

5.2. Hardware Efficiency and Byte Representation

One of the most significant implications of this study is the 50% reduction in physical channel requirements. As demonstrated in the architectural analysis, a single ESU encodes 2 bits of information. Therefore, a group of four units can process a full 8-bit byte simultaneously. In high-density data buses, this reduction directly translates to lower power consumption and simplified PCB routing without sacrificing data integrity.

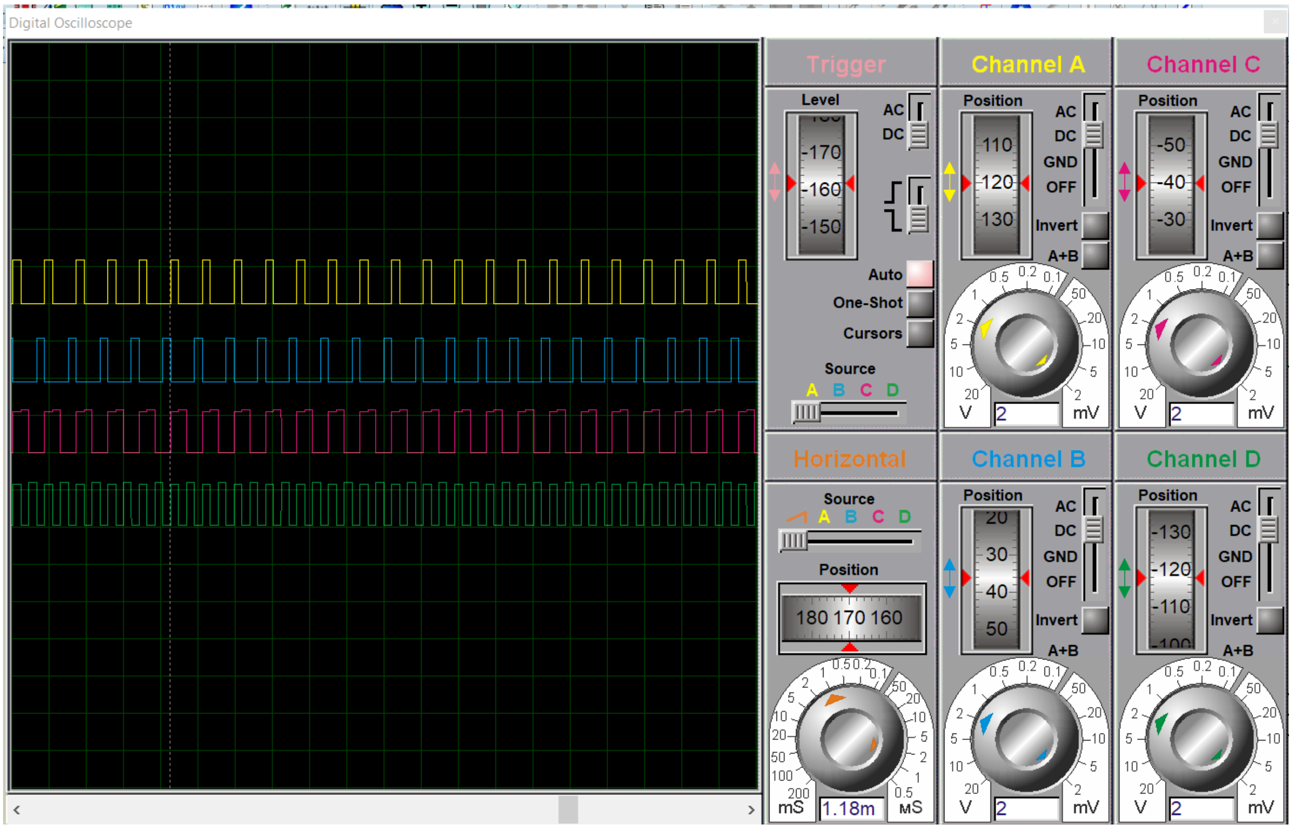

Figure 8: *Timing analysis showing the deterministic transition between states. The absence of mid-level voltages confirms the binary-compatible nature of the ESU's quaternary output.*

5.3. Physical Embodiment: The Mechanical Domino Model

To further validate the universality of the ESU logic, a physical 'Domino' or 'Rotating Cube' model was conceptualized. In this model, the four relational states (N, P, A, X) are represented by the distinct faces of a rotating element. This physical embodiment serves as a proof-of-concept for non-electronic execution, illustrating that ESU logic can be implemented via any medium capable of representing four exclusive states—including mechanical rotations or, more significantly, optical spectral modes.

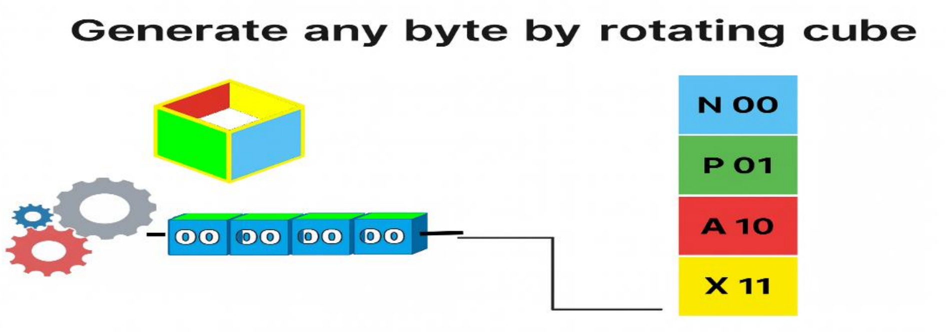

Figure 9: The mechanical ESU model. Each cube represents a 2-bit relational unit; the synchronization of four such cubes visually represents the formation of a full 8-bit byte through parallel state-mapping.

5.4. Toward Spectral Transmission (Future Outlook)

The transition from binary logic to the ESU’s quad-state representation paves the way for the next evolution in communication protocols: **Spectral Parallelism**. By mapping these four states to specific optical wavelengths (RGBY), data transmission speeds can be theoretically increased by 800%. This study provides the necessary hardware foundation to transition from traditional serial/parallel electronic buses to high-speed, multi-valued spectral fiber-optic networks.

5.2 (Hardware Efficiency):

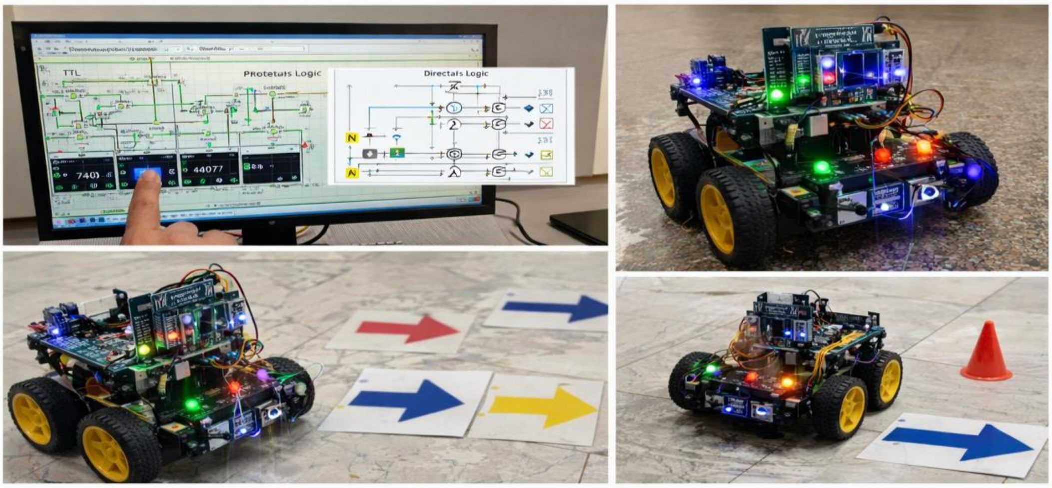

Figure 11: Ròbohics prototype demonstrating the ESU's practical utility

The unit's ability to process complex directional logic with reduced wiring was showcased, proving that the 50% hardware reduction directly benefits compact embedded systems like

6. Future Implementation: Toward a Spectral Byte-Optical Link

"Building upon the successful validation of the ESU, ongoing work is focused on integrating four synchronized ESU units into a high-speed optical transmission system. This upcoming architecture employs four independent fiber-optic channels, each modulated by a unique spectral state. At the receiving end, a specialized **'ESU_back'** cell is utilized, incorporating four **TCS3200 color-to-frequency sensors** acting as spectral analyzers. These sensors are calibrated to detect and decode the RGBY-k3l relational states in real-time.

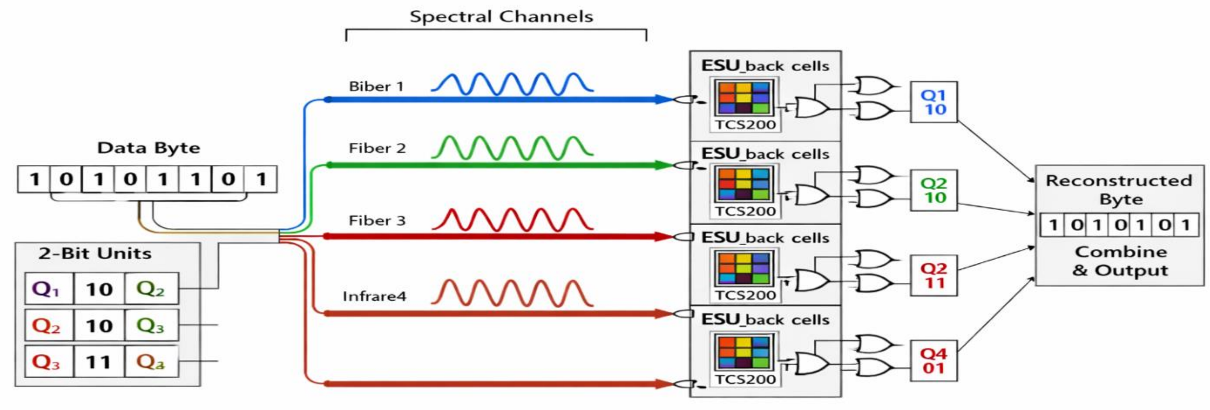

Figure 10: Conceptual diagram of the synchronous spectral link

The byte is split into four 2-bit units, transmitted as distinct spectral signatures across four fibers, and reconstructed instantly by the TCS3200-based ESU_back cells.

As a definitive technical conclusion, the synchronization of these four spectral cells allows for the transmission of a **complete 8-bit byte in a single temporal pulse**. By exploiting spectral parallelism instead of serial binary pulses, the system achieves a theoretical throughput increase of 800%. This closed-loop configuration (ESU-Front to ESU-Back) marks the transition from traditional electrical buses to the first generation of parallel-synchronous spectral data links."

7. Conclusion

This study has successfully demonstrated the physical realization of the **Executable Spectral Unit (ESU)**, a novel architecture that bridges the gap between theoretical Multi-Valued Logic (MVL) and practical digital hardware. By shifting the logical paradigm from absolute voltage thresholds to **relational polarity**, we have eliminated the instability and noise sensitivity that have historically hindered MVL implementation.

The experimental results, validated through Proteus simulations and high-frequency oscilloscope analysis, confirm that the ESU provides a robust, non-overlapping four-state logical space using standard TTL components. The transition from binary to quaternary representation allows for a 50% reduction in hardware channels, effectively enabling four units to process a complete 8-bit byte.

Furthermore, the conceptualization of the **'Domino' mechanical model** proves the medium-independent nature of this logic, while ongoing developments in **TCS3200-based spectral analysis** point toward a new era of optical communication. We conclude that by utilizing four synchronized fiber-optic channels and **ESU_back** recovery cells, it is now possible to transmit an entire byte within a single temporal pulse. This achievement represents a fundamental leap toward a **parallel-synchronous spectral protocol**, offering a theoretical speed enhancement of 800% and setting a new benchmark for next-generation data transmission networks."

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